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COMPUTER RELAYING

A CONTINUING EDUCATION SERVICE
OF THE IEEE POWER ENGINEERING SOCIETY

TABLE OF CONTENTS

CHAPTER		PAGE
-	CONTRIBUTORS	3
-	FOREWARD	4
I	INTRODUCTION TO COMPUTER RELAYING	5
II	SIGNAL CONDITIONING	9
III	ALGORITHMS FOR PROTECTIVE RELAYING	16
IV	LINE RELAYING I	29
V	LINE PROTECTION II - UNCONVENTIONAL APPROACHES	40
VI	PROTECTION OF GENERATORS USING DIGITAL COMPUTERS	51
VII	TRANSFORMER DIFFERENTIAL PROTECTION	60
VIII	RELAY SYSTEMS AND HARDWARE CONSIDERATIONS	67
IX	BIBLIOGRAPHY OF DIGITAL COMPUTER RELAYING LITERATURE	74
-	BIOGRAPHIES OF CONTRIBUTORS	78

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FOREWORD

Computer relaying developments stretch back over at least 12 years. While digital hardware has found its way into commercial products, the stored-program processor has not yet been applied except in a few trial installations. It appears, though, that microprocessor systems may now be cost competitive with some of the more sophisticated dedicated-hardware protective relaying systems.

The material for this tutorial has been especially prepared by highly knowledgeable experimenters in this field. It has been carefully integrated as a sound basis for a full-day tutorial which includes a comprehensive treatment of substation applications in addition to generator protection and general requirements for computer hardware and software.

My earliest recollection of this subject dates back to almost 1965 when the Idaho Power Company suggested that load shedding and out-of-step relaying could be best handled by a central system-operations computer. Both of these functions have aspects which can transcend the information available at a few stations; they are system problems, rather than protection-zone related. There is very little in the literature on these computer applications; they are <u>not</u> covered in this tutorial.

Computer relaying started in the era of minicomputers. Some early work considered the use of a central substation computer that would handle all the station relaying. Based on the hardware then available, it was logical to consider this as one possible approach. Now, however, the microprocessor technology has seemed to still all debate, with decentralized, parallel processors the only solution being considered for high-speed fault protection. With this approach, the central substation computer would be relegated to mostly non-relaying functions and an intermediate link between the microprocessors and the central system-operation computer complex.

The use of a multitude of microprocessors seems essential for acceptance of the technology by utility protection engineers who I think correctly oppose "putting all their eggs in one basket". Another key advantage of many small computers is the much higher unit volume generated. Here the point is related more to the software costs than it is to hardware. Hardware development costs can largely be borne by other appplications; whereas, software costs must be borne by the protective-relaying industry. This industry is characterized by a very low volume, particularly in the more sophisticated transmission line applications. The industry cannot afford to develop and maintain central substation packages. By providing a multitude of processors on a protective-zone basis, the software costs can be reduced and spread over many units.

In 1971, the Power System Relaying Committee established a Computer Relaying Subcommittee. All of the participants in this tutorial have been associated with the activities of this subcommittee, some from inception. Perhaps surprisingly, it was disbanded in 1978. The committee felt that it was time to integrate their activities into the mainstream: active working groups covering computer applications are now part of the Rotating Machinery Protection, Line Protection and Relay Input Sources Subcommittees. The objective is to spur cross-fertilization between the researchers and users. The committee reorganization probably signals imminent commercial realization of the stored-program computer to the vital area of power-system protection.

As Vice Chairman of the sponsoring committee and as a former experimenter in this field, I hope you find this tutorial most beneficial.

George D. Rockefeller
April 18, 1979

CHAPTER I

INTRODUCTION TO COMPUTER RELAYING

This course will deal with recent developments in the field of digital computer relaying of electric power equipment. It is well known that the electric utility industry is among the most dedicated users of large digital computers. In fact, this industry has been one of the earliest users of the computer as a basic tool of engineering analysis. Some of the largest production programs in existence today are power system analysis programs. Application of small process control computers in the electric utility industry is a relatively new development. An example of such an application is the computer based control and data acquisition system. These computer based systems are handling many sophisticated power system operations problems, including State Estimation, Generation Control, Economic Dispatch of Generation, etc. Small computers are also being used in many Supervisory Control systems.

The appearance of process control computers on the market has given an impetus to their case in many industrial systems. These computers are smaller in size, more rugged, and have smaller operating systems than their mainframe counterparts. Their peripheral devices include more analog and digital Inputs/Outputs, and their file-handling systems are likely to be stripped down versions designed to meet the needs of the specific application. Earlier process control computers were mini-computers, while the modern ones tend to be micro-computers. The distinction between mini and micro-computers seems to become less obvious as time goes on; although in the present context the two classes of computers are meant to imply a cost and size difference of an order-of-magnitude.

Use of digital computers for protection of power system equipment--relaying--is an idea of quite recent origin. A great deal of research is going on in this field. Although there are some indications of what the future of these systems will be, as yet there are no completed commercially available protection systems offering relays based on digital computers. This is a new, exciting, changing field. New ideas are being presented regularly in the technical literature. For a Research and Development engineer, this is a challenging and rewarding field to work in. It can be asserted with confidence that the ideas being developed in this field--and presented here during this course--will be incorporated in the protection systems of the future.

This first lecture is a general introduction to the subject of computer relaying. A review of the historical background of the subject will be followed by a discussion of the incentives for development of computer based relays. Finally, the major components of computer relaying system will be identified, and a brief summary of the topics covered during the following lectures will be given.

HISTORICAL BACKGROUND

In a remarkable paper[†] [7], Rockefeller undertook the study of protection of all the power equipment in a substation with a digital computer. For a speculative piece of work without any supportive experimental data, the paper is surprisingly comprehensive. It goes into substantial detail of the relaying program organizations and clearly recognizes the problems and bottlenecks associated with such a project using process control computers available at that time. In hindsight, it seems clear that a single computer for the protection of all the equipment in a substation--with redundancy provided through duplication--is not a viable concept in view of the presently available computer hardware. However, several achievements of the paper still stand. Almost all the benefits expected of a computer based relaying system enumerated in Rockefeller's paper are as they are perceived today. If anything, the economic picture for the digital technology vis-a-vis the conventional relaying equipment has changed even more rapidly than anticipated in the paper. More about these economic considerations later.

Other investigators had also begun to consider digital computer based relaying at about the same time that reference [7] was published. In two papers [19, 21] with a somewhat limited scope--that of developing algorithms for the protection of transmission lines with a digital computer--Professor Morrison and his colleagues presented rather complete computer programs, and, what is more important, the authors obviously had specific computer hardware in mind for the implementation of their program. The problem of providing for the protection of a transmission line against any of the several faults that may occur on it was solved by providing a fault classification routine. This classification program performed a rather simple check of voltage wave-forms, and the time consuming impedance calculations were deferred until the fault type was securely classified. The techniques presented in these papers could be accommodated on the then-available process control minicomputers. Essentially similar techniques were used in two development systems: the Westinghouse and Pacific Gas and Electric project reported by Rockefeller et. al. [24, 25], and the American Electric Power project reported by Phadke et al [55,62]. Both of these installations were tested in the field; although neither system used the computer based relay for actual protection of the transmission line. A great deal of practical experience was obtained from these installations.

Of all the computer relaying topics, transmission line relaying has attracted more researchers than any other subject. This is so for several reasons. Transmission line protection is computationally more complex, and thus is a significant test of a computer's capability; furthermore, the high cost of conventional transmission line relays makes this a worthwhile problem to tackle. More will be said about the transmission line relaying in one of the later lectures. An important variant of the transmission line relaying algorithm was proposed by Professor Morrison et. al. [16], and by M. Poncelet [29]. This approach attempts to solve the differential equation of the faulted circuit. A similar technique was recently implemented by the General Electric Company and the Philadelphia Electric Company [66] in an important project involving minicomputer-based distance relays for the two ends of a 550 kV transmission line. Some of the other centers of significant research in computer relaying are at the Imperial College in London where Professor Cory and colleagues have published a number of papers in this area [13, 18, 63, etc.], the University of Calgary--Professor Hope and

[†] For numbered references, see Bibliography at the end of this text.

colleagues [20, 22, etc.], the University of Saskatchewan--Professor Sachdev and colleagues [27, 34, 36, etc.] and the University of Missouri-Professors Walker, Tudor and colleagues [5, 9, 10, etc.]. In addition, most of the major manufacturers of electric utility equipment in Europe and Japan have active projects on digital computer based relays. Several Electric Power Utility organizations such as the Bonneville Power Administration, the Pacific Gas and Electric Co., the Philadelphia Electric Co., the Pennsylvania Power and Light Co., have had active computer relaying projects. The American Electric Power Co., with which this author is associated, has had a major project in this field since 1970. If one looks at recent technical papers sponsored by the Power System Relaying Committee of IEEE, it is clear that digital relaying is a subject which continues to inspire a large number of researchers. A project was recently funded by the Electric Power Research Institute in this field and surely this is an indication of the great value placed by the Electric Utility Industry on this topic.

EXPECTED BENEFITS OF A DIGITAL PROTECTION SYSTEM

Considering the extensive research going on in the field of digital computer relaying, it is worth considering the benefits that are expected to follow from the adaptation of digital relaying techniques. Although early workers in this field considered the use of a single computer (a minicomputer) for all the relaying functions within a substation, the present view is that the proper approach to this problem is to use a number of microcomputers dedicated to the individual relaying tasks. These microcomputers are to have data exchange facility among themselves: some form of networking of the microcomputers is definitely being considered. Through this networking concept, it is expected that the main advantage of a single computer system--shared data between relays--can be realized without the attendant drawbacks of a central relaying computer.

The most important perceived benefits of a digital relaying system can be summarized as follows:

(1) Economics:

In the final analysis, this will be the most important consideration. The cost of digital hardware has been steadily decreasing. The cost of conventional relaying has increased steadily during the same period. For example, a relaying task that required a $100,000 minicomputer in 1970 can now (1979) be handled by a $10,000 microcomputer. Contrast with this the cost of a typical transmission line protection system which has approximately doubled from 1968 to 1978. Admittedly this takes no account of the software development costs for the computer relay. Although these are high--as with the development costs of any new device--these will be distributed over many similar units. Furthermore, the digital computer, being a programmable device, can be used to perform multiple functions. To the extent that this can be done without jeopardizing the security of the individual tasks, the economic comparison becomes even more favorable to the digital technology.

(2) Performance:

It is expected that in all cases the performance of a digital relay will be at least equal to that of its conventional counterpart. Certain characteristics of a relay--for example the relationship between the optimum speed and reach of a distance relay--are determined by the power system itself, and not by the hardware used to implement the relay. For such functions, the digital relay can be designed to obtain the best possible performance--which is usually equal to that of a well designed conventional relay. On the other hand, certain features come more naturally to a digital relay--for example memory action, complex shaping of operational characteristics, etc.--which lead to a better digital relay than the corresponding conventional relay.

(3) Reliability:

One of the most significant advantages of a digital relay--perceived in the earliest technical papers--is the fact that the digital computer is continuously active, consequently a very high order of self-diagnosis is going on continuously within a digital relay. Additional diagnostic features--such as the monitoring of many of its peripherals--can be easily programmed. It is therefore expected that most of the accidental failures within a digital relaying system can be detected immediately, and appropriate corrective actions taken. Although some diagnostic functions are usually available in a conventional relay, this feature can be utilized in a digital relay with a high degree of sophistication.

(4) Flexibility:

Being a programmable device, revisions or modifications necessitated by changed operating conditions can be made in-place rather easily through different pre-programmed memory modules. It is also conceivable that a common hardware system can be developed which will serve as one of several relays--again through different pre-programmed memory modules. This should lead to a smaller inventory for repair and maintenance tasks. In some relays, where some or all of the input signals are identical, alternate input paths can be provided. The alternate paths would be unused under normal system conditions, and can be activated under program control when trouble develops in the normal input paths. This flexibility in the routing of input data leads to a higher level of reliability for a given amount of hardware.

(5) System interaction:

At present, there are a number of sub-systems in electric utility substations which exchange data with remote locations--usually a control center. An example of this is the alarm system, using either a simple scheme with two alarm codes--supervisory and maintenance alarm--or more elaborate alarm systems furnishing additional descriptive information. Another example is the data acquisition system, which utilizes remote units in a substation, and obtains system operational data--such as power flows--for a central dispatch center. A supervisory control system is a third example of such a subsystem. In all of these systems, there is a need to communicate between a remote location and a substation. With the existence of computers within the substation, handling of these communication functions can be integrated into a single communication system. Some modes of remote interactions which can not be foreseen in today's technology, may become practical in the future when the possibility of communicating with the individual relays is realized.

(6) Byproducts:

When a computer based relaying system is considered, other totally new applications become realizable which have no parallel in existing technology. Several examples of this can be given now, although almost certainly far more interesting ideas are likely to occur in the future as experience with these systems is accumulated. For example, a computer relay can furnish post-fault analysis of all observed transient phenomena.

A distance relay could furnish the computed distance to a fault immediately after the occurrence of the fault. This information could be used by maintenance personnel for faults which are of a permanent nature and require transmission line maintenance. An exhaustive sequence-of-event analysis can be furnished locally or to a remote location by exchanging the post-transient data between several relaying computers. Another instance is the data-multiplexing activity--which exists in some isolated cases in today's technology--but because it comes naturally to a digital data stream, a great many more data may be multiplexed with computer based substation protection systems. This will of course help reduce cabling expenses between the station yard and the control house. Yet another example of such a byproduct comes about from the low burden presented by computer based relays to the transducers as compared to that presented by electro-mechanical relays. Low burden current and potential transformers using modern electronics and fiber-optical medium for data transmission from high voltage apparatus to ground potential have been discussed in the technical literature during recent years. A relay that places low burden on the transducer is a natural mate to such a transducer; and would give a new impetus to the commercial development of the transducers. Considering the high costs associated with conventional HV and EHV transducers, a successful development of such a unified protection system may turn out to be the most important byproduct of all.

FUNCTIONAL BLOCK DIAGRAM OF A COMPUTER RELAY

Figure 1 is the functional block diagram of a digital computer based relay. Depending upon the specific relaying function being implemented, some functional blocks may be more or less significant compared to other functional blocks. However, in almost all relaying systems being considered in this course, this functional description is applicable. The only exceptions are some of the novel distance protection systems for transmission lines which will be described in one of the later chapters.

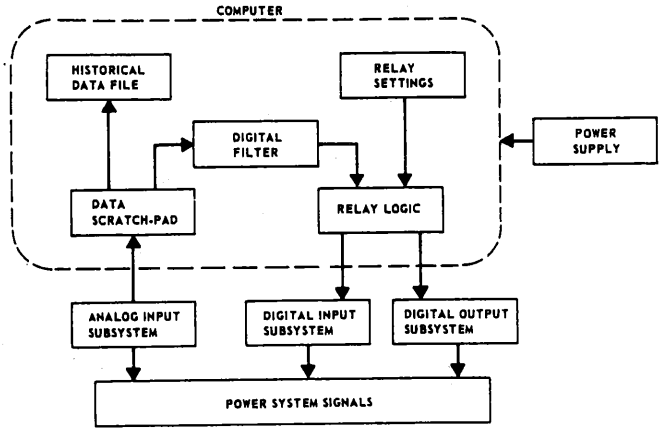


Figure 1
Functional Block Diagram of a Digital Relay

The inputs to the relay computer are analog and digital signals derived from the power system. The analog signals consist of power system currents and voltages--primarily 60 Hz quantities in steady state. The number of analog signals needed depends upon the relaying function. A distance relay, for example, requires a minimum of three phase currents and three phase voltages. A bus differential relay on the other hand may require as many as fifteen current inputs if there are five circuits connected to the bus. Thus the number of analog inputs to a digital relay should be considered to be highly function dependent. Perhaps the number of analog signals lies between 3 and 30 in all cases.

The primary analog signal levels are very high--measured in kiloamperes and kilovolts. The traditional transducers reduce these signals to low levels (for example: five amperes and sixty-seven volts line to neutral) at ground potential. Certainly one approach for digital relaying applications--in fact the only one used in practice so far--is to take the secondary signals from these transducers as inputs to the relays. These signals must be further attenuated to acceptable computer input levels--usually ±10 volts maximum. This level reduction must be accomplished by circuits which shield the computer from transient voltages that exist on the secondary leads. The shielded and attenuated signals are then converted to digital form by Analog to Digital converters. All of these functions are performed by the Analog Input Subsystem shown in Figure 1.

The Digital Input Subsystem handles the contact or voltage sense information needed by the relays. On most relays, the number of digital inputs is of the order of five to ten. The digital input signals are status changes ('on' or 'off') of isolated contacts; or changes in voltage levels (for example: +48 V and 0 V) in a circuit. In the case of isolated contacts, an auxiliary power source and sensing mechanism must be provided to sense the status of the contacts. As in the case of analog signal wiring, there are transient voltages on the digital input wiring also, and shielding of computer input ports from these voltages, as well as the provision of buffer power supplies where necessary, is the function of the digital input subsystem.

The output of a digital relay is through its digital output subsystem. A maximum of five to ten digital outputs are sufficient for most relaying application. Computer digital outputs are usually from its parallel-output port, and in most cases these are TTL level signals. These signals are buffered, and a suitable current or voltage level is derived from the computer generated TTL output by the Digital Output Subsystem.

The analog data is sampled continuously, the sampling rates varying between 240 Hz to about 2000 Hz as described by various authors. The continuously generated sample set is entered into the computer memory, either under program control or through a Direct Memory Access channel. In either case the data is maintained in a Scratch Pad random access memory (RAM). The memory is organized as a carousel structure, and suitable pointers are maintained for data retrieval.

In most digital relaying applications, the raw data samples are also stored in a secondary data file for historical recording of significant transient events on the power system. The organization and length of this Historical Data File depends upon the user needs and the available RAM. It is understood that this data is moved as soon as possible to a secondary storage, thereby making room for the next occurrence of a transient. A suitable span of prefault data as well as appropriate time-stamps and messages are also saved in this Historical Data File. The final disposition of these files depends upon the details of individual system design. If a host computer with disk space exists in the substation, the historical data is moved to the disk. It may be transferred to a remote host if a telecommunication line exists, or it may be used to produce a hard copy locally. In any case, it is of utmost importance that the historical data files be

purged as quickly as possible.

The digital filter program is essential to all relaying applications. The analog data samples are corrupted by noise from many sources. A power system transient is a very complicated function of time, and a substantial portion of its spectrum is noise as far as the relaying application is concerned. In addition, there may be noise contributed by the A/D converters. In order to obtain accurate results, the digital filter must separate the desired components of the analog signals from the noise components. This function is handled by the Digital Filter Program. In most applications the filter equations are recursive, and much ingenuity is expended in producing very fast digital filter algorithms.

The Relay Logic program determines the functional behavior of the relay. The filtered data is used to calculate secondary quantities which are convenient vehicles for the relay description. A transmission line distance relay characteristic for example is a region in the complex impedance plane. Consequently, the fault impedance, which is the ratio of a filtered voltage and current pair, is the secondary quantity needed by a distance relay program. Similarly, a differential relay requires the calculation of tripping and restraining currents. A harmonic restraining relay requires the computation of a weighted sum of certain harmonics.

These derived (or secondary) quantities are compared against various preset relay characteristics. The size and shape of these characteristics is entered into the computer by the relay setting program. It is through this program that the user--the relay engineer--specifies the desired relay performance.

The power supply to a relay must not depend upon the station ac supply. Consequently, a battery/charger system, and a dc-dc converter is needed to supply power to a relaying computer. From this point of view, a computer requiring dc power at a single voltage level is quite attractive.

The chapters that follow will discuss most of these functional blocks in detail. The second chapter will deal with signal conditioning. This refers to the analog and digital input and digital output of the computer. The attenuation of primary signals to lower levels and A/D conversion will be discussed in this lecture. Special transducers--such as electronic current transformers--will also be described.

The third chapter is on algorithms for digital filtering. As pointed out earlier, one of the main concerns in all relaying applications is the extraction of usable signal from a noisy input source. Digital filtering in relaying applications is characterized by a narrow data window containing relatively few samples. Algorithms specially suited for such applications will be given special attention in this lecture.

The next four chapters deal with specific relaying application programs. This includes generator, transformer, and bus protection. Differential protection schemes will be described; and harmonic restraint function for transformer protection, as well as the negative sequence power relaying of generators will be described. The next two chapters will deal with transmission line protection. The first of the two line relaying chapters deals with conventional multi-zone step-distance relay, while the second chapter describes some recent work on novel relaying schemes--such as wave propagation relays.

The last chapter will cover subjects which are of general interest in the field of digital relaying. An example of such a subject is a review of transmission line distance relaying from the point of view of estimation theory. This leads to certain limits inherent in the distance relaying concept. Such analyses help clarify the goals of a relaying program, and should be carried out before undertaking the implementation of any relay on the digital computer. Next, the hardware needed for the implementation of a digital computer relay will be described. Here again, the distance relay will be taken as an example, and a specific computer structure being planned at AEP for field testing will be described. The lecture will conclude with a consideration of possible hierarchical structure for computer networks within a substation.

CHAPTER II

SIGNAL CONDITIONING

The power system we are protecting is obviously analog in nature. The fault currents and voltages measured on various pieces of equipment and lines must be conditioned and eventually digitized for the computer relay to properly analyze the signals.

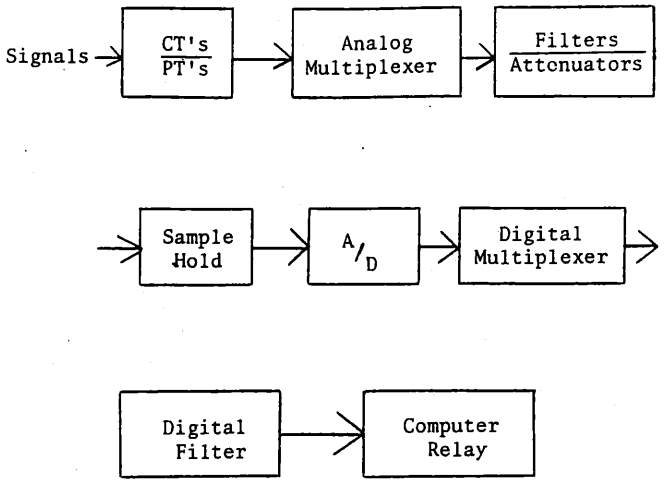


Figure 1

Many technical considerations must be studied when applying signal conditioning subsystems to computer relaying. Some of these considerations are accuracy and resolution requirements, linearity requirements, and calibration stability. Such factors as error resulting from temperature changes, conversion time, and power supply stability requirements must be carefully studied. The nature of the input signal must be fully understood including relative noise levels in order to determine the proper type signal conversion system to use. The type output signal must be known to properly interface with other digital equipment. Unless all of the above factors are properly considered, the potential for error is great in the conversion of analog signals to digital coded information.

The first step in relaying is to secure information from the lines or equipment, a process typically accomplished through the use of current or voltage transformers. The purpose of the current transformer is to properly reproduce in the secondary the current waveform found in the primary. This must be accomplished with a known accuracy and therefore is a function of such factors as the highest secondary voltage which can be produced without transformer saturation. Current transformers are classed according to accuracy as defined by ANSI C37.13. Factors such as the burden placed on the transformer will obviously effect its accuracy. Careful consideration must be given to this and other factors when applying current transformers. Computer relaying systems offer a distinct advantage in that the signal conditioning and input hardware presents a small burden to the current transformers. This allows great flexibility in terms of the amounts and type of equipment which can be served from a given current transformer.

Considerable care must be taken in matching the characteristics of a given transformer to the relaying system. These devices should be studied and fully understood by the computer relaying engineer. A good introduction to the nature of these devices can be found in the Westinghouse Applied Protective Relaying handbook.[59]

Voltage or potential transformers are designed to reproduce in the secondary the voltage waveform found in the primary of the transformer. Voltage transformers are usually assumed to be high accuracy devices capable of good transient response. An exception are those devices using coupling capacitance. The transient response of these devices may significantly vary from the primary input and may even be oscillatory.

Again, these devices should be fully understood prior to the application of computer relaying. An introduction to voltage devices can be found in the book Applied Protective Relaying.

Since these current and voltage transformers are the primary sources of information from power lines and equipment, it is necessary that any computer relaying system be able to use the data presented from these devices. Many computer relaying techniques which depend on 60 Hz information or the fault information contained in lower order harmonics will have no problem with these devices. However, certain relaying techniques which need high frequency data may find the standard current and potential devices inadequate in terms of high frequency response or transient behavior. Much work remains to be done to determine the adequancy of standard current and potential devices for all proposed techniques of computer relaying.

Current and potential transformers have standard secondary voltage and current levels. These are primarily 5 amps and 120 volts. While these are the standard input ranges for most commercial protective relays, they typically are not appropriate for the circuits found in computers. It is therefore necessary in many cases that voltage and/or current waveform amplitude attenuation take place. Given the low burden requirements of the computer relaying input circuitry, it is a relatively easy task to condition these input waveforms. For example, in the case of current inputs it is possible to design a current amplifier circuit which will simultaneously define a fixed burden to the current transformer and reduce the current amplitude to acceptable current levels. Since the circuit concepts required to perform these functions are generally understood, they will not be investigated at this time.

A special problem occurs when the computer relaying system requires high accuracy during both normal and high level fault conditions. The problem can be resolved by proper application of the analog-to-digital converter systems but it can also be handled in the input circuitry. A satisfactory solution for some computer relaying applications is the use of nonlinear amplifiers (e.g. logarithmic, etc.). The transfer function of such devices is nonlinear and results in a degree of compensation for the broad dynamic range between normal and fault current values. The input system of the computer relay must be designed to accept this nonlinear input. This represents only one possible solution to the problem of broad dynamic range and obviously is appropriate for only a limited number of computer relaying systems. Again, the electronic circuitry required to perform these functions is well understood. Numerous references in electronic and instrumentation texts satisfactorily describe this type circuitry. It is usually assumed that in modern hardware applications the input signal conditioning and

amplifier circuits will be of integrated circuit design. We recommend the text Introduction to Operational Amplifier Theory and Applications as an introduction to this type electronic design.[39]

According to the data requirements of the particular digital relaying technique being implemented, it is sometimes necessary to do analog filtering of the data received from current and potential transformers. The purpose of this analog filtering is to permit the transfer of certain frequencies in the input signal and to attenuate other frequencies. For example, a digital relay which is to be used to detect overcurrent conditions of the 60 Hz waveform may require heavily filtered current signals such that only the 60 Hz fundamental is presented to the relay. An analysis of the input data requirements of various types of relays will follow.

In general, filters may be broken into four classes: high-pass, low-pass, bandpass, and band-reject. The transfer characteristic, $|A_V(f)|$, of an ideal high-pass filter is shown in Figure 2, and an ideal low-pass filter in Figure 3. In an ideal high-pass filter, all frequencies above a cutoff frequency are transferred with no attenuation and all frequencies below the cutoff frequency are attenuated to zero.

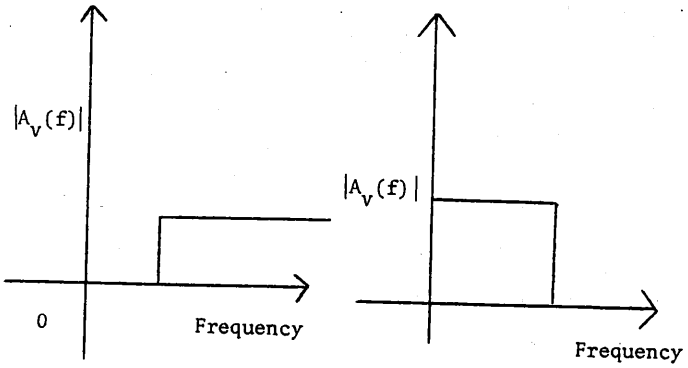


Figure 2

Figure 3

Conversely in an ideal low-pass filter the frequencies below a cutoff frequency are transferred with no attenuation, and the frequencies above the cutoff frequency are attenuated to zero. Of course, it is impossible to attain these ideal transfer characteristics using physical components but these transfer characteristics may be approximated. The transfer function of almost any high-pass or low-pass filter of any order may be expressed as the product of first order and second order transfer functions.

Bandpass filters and band-reject filters are combinations of a high-pass filter and a low-pass filter. An ideal bandpass filter has a transfer characteristic as shown in Figure 4. In this case a band of frequencies is transferred and frequencies higher and lower than this band are attenuated. This may be done by cascading a high-pass filter with a cutoff frequency of f_1 and a low-pass filter with a cutoff frequency of f_2, which will allow only frequencies between f_1 and f_2 to be transferred. An ideal band-reject filter, or notch filter, has a transfer characteristic as shown in Figure 5. This characteristic may be obtained by using the approach shown in Figure 6, in which the same input is applied to a high-pass filter with a cutoff frequency of f_2 and a low-pass filter with a cutoff frequency of f_1 and then summing the outputs of these two filters. In this way only the frequencies between f_1 and f_2 are attenuated.

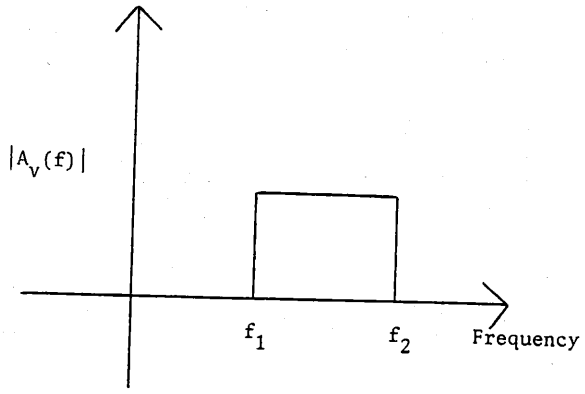


Figure 4

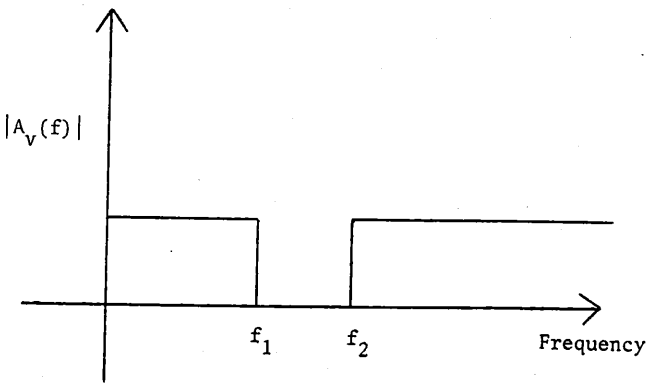


Figure 5

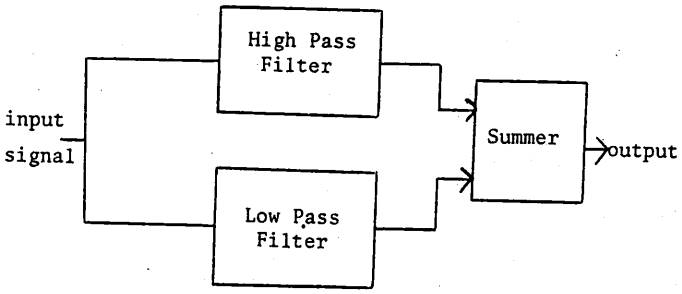


Figure 6

In addition to the steady state characteristics of filters, the dynamic response of the filters should also be taken into consideration for any given application. Probably the most important of these dynamic characteristics are the rise time, which gives an indication of how long it takes a low-pass filter to reach its final value; the overshoot, which is an indication of how much a second order filter will exceed its steady state value on the initial response to a step input; and the settling time, which is an indication of how long it takes a second order filter to settle to its steady state value.

It is necessary that considerable attention be

given to the analog prefiltering of current and voltage information before presentation to the digital relay. One must have a thorough understanding of the affects of various frequencies on the relaying algorithm and an understanding of the information content of the fault waveform at various frequencies. These considerations will be discussed in detail in the section on data sampling and in the discussion of individual digital relaying algorithms.

A multiplexer is a device which selects a signal from one of its two or more input channels and transfers this signal to its output channel. A solid state multiplexer may be modeled mechanically by a multiterminal rotary switch. With suitable accompanying circuitry, a multiplexer allows the transmission of several signals over a single communications channel. Thus, multiplexers are found in a wide variety of applications, including data acquisition, data distribution, parallel to serial data conversion, and many others.

For digital relaying applications involving multiple analog signals, it is sometimes necessary to use an analog multiplexer. An analog multiplexer permits a single output line to mirror the signal at the selected input channel. Thus, the multiplexer is essentially a collection of analog switches (Figure 7) controlled by the necessary channel selection logic.

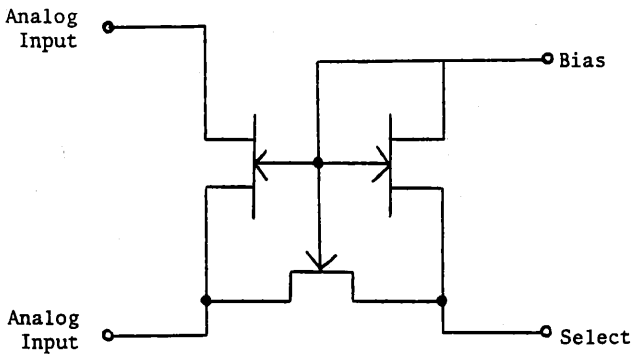


Figure 7

The selection is performed in the manner previously discussed: a binary code is supplied to the multiplexer whose internal logic circuitry connects the output to the corresponding input channel. The signals applied to the input channels may be either single-ended (referenced to the system ground) or differential (two terminals required). Single-chip analog multiplexers are available which provide up to 16 single-ended or 8 differential input channels. A chip disable control line is included to permit parallel expansion if external logic is utilized to select the desired multiplexer. Unlike digital multiplexers, however, the accuracy of an analog multiplexer is dependent on the load impedance presented to the output terminals. The load impedance is often recommended to be 10^8 ohms or more to achieve maximum accuracy. This rarely creates a problem, however, since analog multiplexers are typically used to drive IC operational amplifiers or IC sample-holds, whose input impedances are in the range of 10^8 to 10^{12} ohms.

A frequent application of analog multiplexers is depicted in Figure 8. In this configuration, only one sample-hold and analog-digital converter combination is required to digitize the eight analog input signals. A separate sample-hold and analog-digital converter would be required for each input signal if the analog multiplexer could not be utilized.

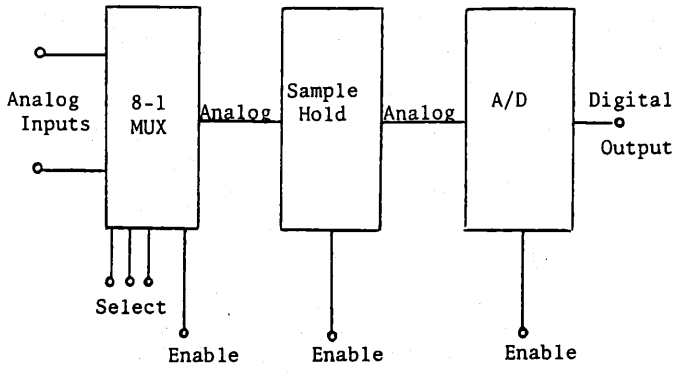


Figure 8

Digital multiplexers are available in all logic families and merely sense whether the input voltage is HIGH or LOW (+5 or Ø for TTL and CMOS, Ø or -5 for ECL). The output voltage is then controlled to maintain the same logic level or its complement, depending on the specific design technique utilized. A simple 2-input, 3-bit multiplexer could be constructed as shown in Figure 9. In this configuration, a HIGH voltage level at SELECT A and a LOW voltage level at SELECT B would result in the transfer of the three bits of data on channel A to the three output lines. Alternatively, a HIGH level at SELECT B and a LOW level at SELECT A would transfer the data on channel B to the output. Obviously, the possible combinations of number of input channels and number of bits per channel is infinite. Commercially, multiplexers are available in single chip packages which range from 2-input, 8-bit to 16-input, 1-bit. In addition, two or more multiplexers may be

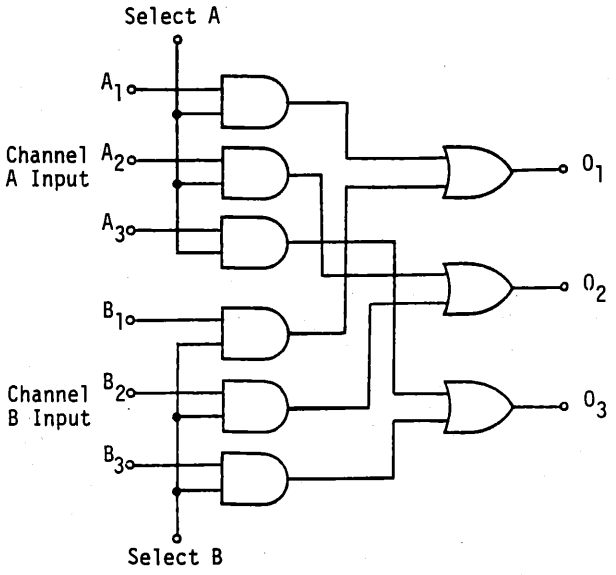


Figure 9

combined on a single chip for some configurations, such as quadruple 2-input, 1-bit. For multiplexers with more than two input channels, it becomes undesirable to have a separate select line for each channel. Since digital systems only recognize two voltage levels, the optimum solution is to utilize a binary code to select the appropriate input channel. In order to simplify the associated circuitry, each multiplexer chip also incorporates the logic necessary to decode these binary channel selection codes. In addition, most multiplexers furnish an additional control line which can be used to disable the output lines. Thus, the output may be disabled when it is desired to communicate with another device using a common data bus. For this reason, most digital multiplexers have three-state outputs, allowing the output lines to assume a high impedance when they are disabled. This prevents the output lines from affecting the data bus when they are disabled. In addition, the output disable allows several multiplexers to be paralled to increase the total number of input channels. External logic is required, however, to disable the output of each undesired device. A typical application of digital multiplexers incorporating all of these features is shown in Figure 10. This configuration allows a microprocessor to access a variety of data sources which share a common data bus. A second multiplexer serves a parallel-to-serial converter and allows the microprocessor to transmit data to a teletype or similar piece of equipment.

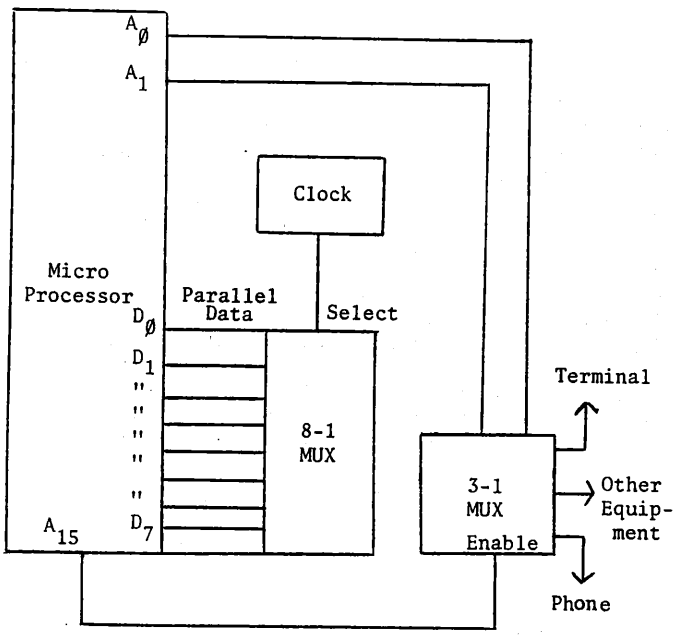


Figure 10

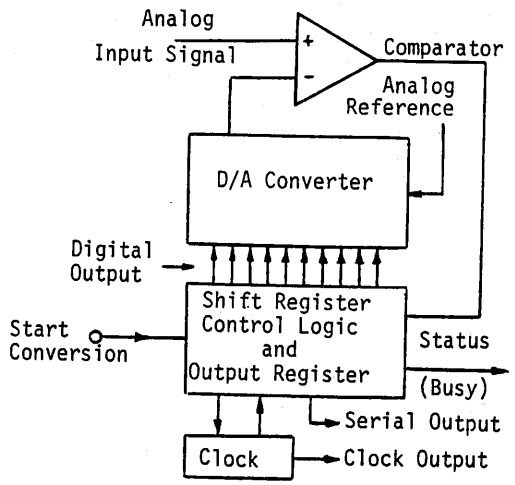
Many techniques have been developed for converting analog electrical quantities to corresponding digital representations. The approaches are so numerous that only those methods most frequently implemented will be discussed. Currently, most methods of A/D conversion will fall into one of the four categories:

a) Successive Approximation
b) Integration
c) Counter and "Servo" Types
d) Parallel and Modified-Parallel Types

The basic principles involved in each of these techniquos play an important role in the data acquisition design scheme, since a thorough knowledge of the method implies a knowledge of its limitations.

All bits of the digital represention are initially set to zero. A comparison is made between the digital representation, with the most significant bit set high, and the analog input, using a digital to analog converter (D/A) and a voltage comparator. If the digital representation translates (through the D/A) as a higher value than the input, that bit is set to zero. This process proceeds, setting the next bit high etc., until each bit from the MSB to the LSB is run through the comparison process. The end result is the desired digital representation.

Accuracy, linearity, and speed are primarily affected by the properties of the D/A converter (and its reference), and the comparator. In general, the settling time of the D/A converter and the response time of the comparator are considerably slower than the switching time of the digital elements.

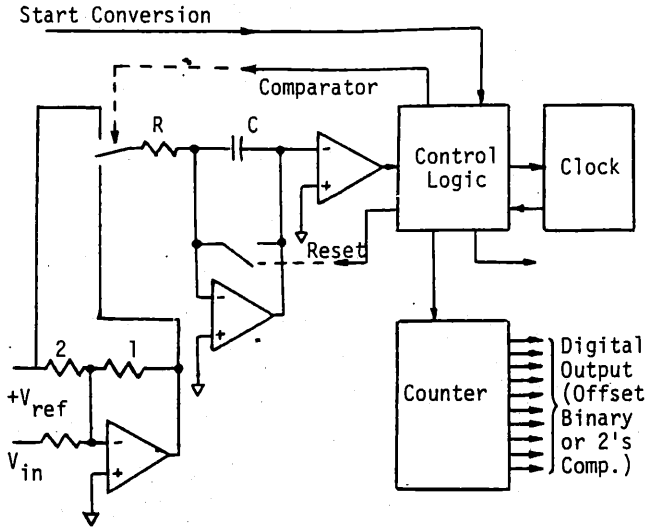


Successive-Approximation A/D Converter

Figure 11

All integration techniques are related in that a counting sequence over a period of time determines the digital representation. The dual-ramp type integrates the sampled analog signal for a specified period of time, charging an internal capacitor. A reference voltage is then integrated in opposition to the existing charge on the capacitor while a counter records the time required for the capacitor to be discharged. The final count is the desired digital representation. Conversion accuracy is independent of both the capacitor value and the clock frequency, because they affect both the up slope and the down ramp in the sampling period.

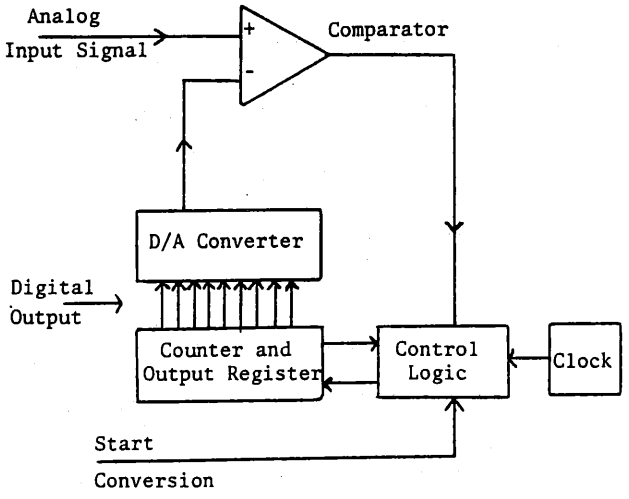
Other conversion approaches in this class include the single-ramp type and voltage to frequency converters. In the single-ramp converter, a reference voltage, of opposite polarity to the signal, is integrated until the output of the integrator is equal to the signal input. Hence, the single-ramp converter is similar to the dual ramp method; the weakness is that its accuracy depends on both the capacitor and the clock frequency. In the V/F converter, a frequency is generated in proportion to the input signal; a counter measures the frequency and provides a digital output code, the value of which is proportional to the input signal.



Dual-Ramp A/D Converter

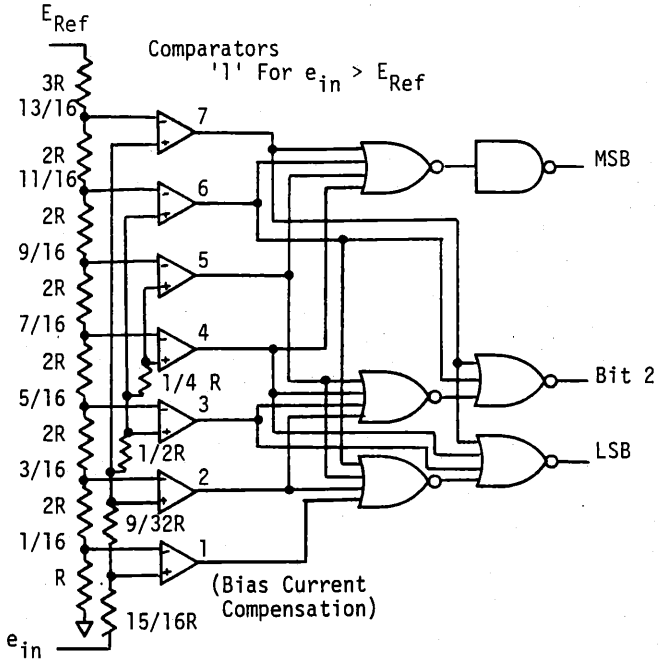
Figure 12

Counter type A/D's are simple in concept. A count is initiated and used to drive a D/A, the output of which is compared to the input until the two are equal, whereupon the count is ceased. This converter has the disadvantage of limited speed for a given resolution, since the conversion time for a full-scale change is equal to the clock frequency divided into the maximum number of counts. The "servo" type is similar except that the counter may count up or down and, therefore, tracks the analog input and can follow small changes quite rapidly.



Counter-Comparator A/D Converter
Figure 13

The parallel type A/D exhibits the fastest conversion rate currently available from the essential types of A/D's. The reason being that a comparator exists for every possible digital representation. As the input increases, an increasing number of comparators switch on. Digital logic then converts the comparator outputs to a digital code representing the analog input. The disadvantage of this technique results from the geometrically increasing number of comparators as the bit number is increased, which contributes greatly to cost as higher resolution is required.



Parallel 3-Bit A/D Converter
Figure 14

Combinations of the procedures outlined above frequently allow new levels of performance to be achieved. For example, by combining parallel conversion for small numbers of bits with successive approximation, it is possible to strike a compromise that gives better resolution than a parallel approach, with less complexity, and improved speed over the successive approximation approach.

The particular methods by which digital representation of an analog signal may be generated have been discussed thus far; however, the representation may be accepted in many forms, each with its own advantages. Additionally, the rate at which the conversion process proceeds determines to a great extent the nature of the data acquisition system. These two aspects of the analog to digital conversion process constitute the two main criteria for applying the principles of analog to digital conversion and can be best described in terms of the resolution desired and the sampling or conversion rates necessary to implement a given data acquisition scheme.

The resolution available with any digital representation is a function of the number of available bits and the form of the bit code. Consider for a moment an unsigned binary form of eight bits. The range of values that may be represented extend from 0 to 255, corresponding to all zeroes or low levels and all ones or high levels repectively. Thus, the resolution available is $1/2^8$ or 1/256 of the full scale expectation, i.e. the uncertainty will lie within ± 1/512. If, however, a signed binary form is implemented, two forms of zero are possible, positive and negative, and the resolution is reduced to 1/255. Other digital forms that are commonly applied fall into one of two categories, unipolar or bipolar. Unipolar forms represent magnitudes extending from zero, whereas bipolar forms include negative representations. Examples of unipolar forms include unsigned binary and binary coded decimal. Bipolar forms include sign magnitude

and two's complement. Any text on digital information representation will discuss these various types and their advantages.[33] Thus, many digital forms exist and A/D's are available with 12 bits of conversion and more. Both factors must be considered together when deriving a system scheme.

The other main criterion for application of A/D principles is sampling rate. This affects the signal tracking capability and the multiplexing schemes (if any). Obviously it would be impossible to gain much useful data from a converter which sampled a sixty cycle signal ten times a second. The conversion rate necessary for a given application would depend, therefore, on the allowable tracking error. As far as multiplexing is concerned, a conversion rate slower than the multiplexing rate would be unacceptable. Also, obtaining information regarding the settling characteristics of the multiplexer switch would be advisable in order to determine how soon the converter could sample a given channel and remain within a specified tolerance.

Although the two criteria of resolution and sampling rates constitute the main concerns in applying A/D principles effectively, other concerns should not go without mention.

To fully understand how to apply A/D converters, we need to be familier with digital sampling theory. A discussion of this topic follows.

Figure 15 will serve as an illustration of how an analog signal is captured and converted to a digital signal. Figure 15 (a) portrays the analog signal to be converted. The train of pulses in Figure 15 (b) represents a fast acting switch which connects the data acquisition system to the analog signal for a very short time and remains open for the rest of the period. The result of this operation is identical to multiplying the very short on time of the sampling switch and the signal. The resultant modulated pulse train is shown in Figure 15 (c), where the amplitude of the analog signal is preserved within the signal envelope at discrete times. Replacing the sampling switch with a switch-capacitor combination enables the signal to the stored or held until the next sample pulse. This type of signal acquisition, as illustrated in Figure 15 (d), is known as a sample and hold technique.

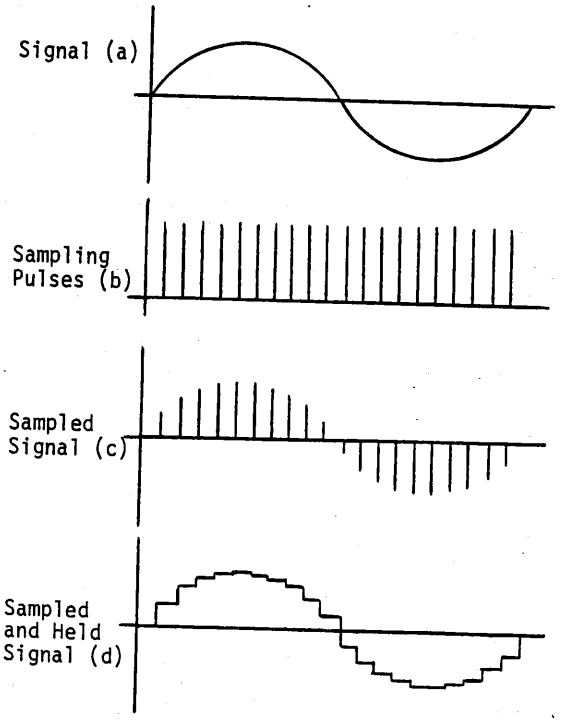


Figure 15

To determine how often the sampling pulses should occur; that is, to determine the "sample rate" for a given system, one must examine the analog signal characteristics. Obviously, the sample rate must be faster than any significant changes in the analog signal in order to retain all the useful information. The Nyquist Sampling Theorem defines a minimum allowable sample rate to be used.[65] It states: If a continuous bandwidth limited signal contains no frequency components higher than f_c then the original signal can be completely recovered without distortion if it is sampled at the rate of at least 2 f_c samples per second. Figure 16 illustrates the sampling theorem. Figure 16 (a) shows the frequency spectrum of the desired signal. If the sample rate is chosen as f_s, then the sampled signal will be modulated by the frequencies in the analog signal, as is shown in Figure 16 (b). Should f_s be less than 2 f_c, the high frequencies of the signals cannot be distinguished from the low frequencies of the sampled signal; thus distortion error exists which is termed "frequency folding."

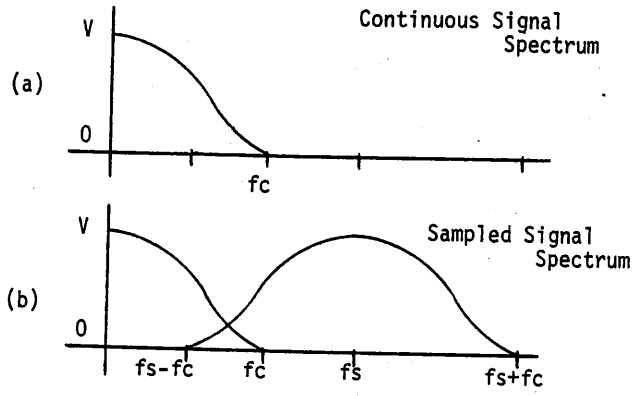


Figure 16

Another error related to a sample rate which is too low is "aliasing". Aliasing error occurs due to the fact that the sampled signal may contain low frequencies that actually do not exist in the original analog signal. This error is seen in Figure 17. The dotted line indicates a low frequency that does not exist in the original signal.

The weight assigned to the least significant bit (LSB) of an analog to digital converter is termed the "nominal resolution" for that converter.[23] The resolution is given in terms of a fraction, a percentage, parts per million (ppm), or in db. A table of the resolutions of the more popular sizes of A/D's

(db is a base ten logarithm of the ratio of the LSB value to full scale (unity) multiplied by twenty.)

follows:

Bits	2^{-n}	$1/2^n$	db	$1/2^n$ decimal	%	ppm
1	2^{-1}	1/2	-6	.5	50	500,000
4	2^{-4}	1/16	-24.1	.0625	6.2	62,500
8	2^{-8}	1/256	-48.2	.0039	.4	3,906
12	2^{-12}	1/4096	-72.2	.0002	.024	244
16	2^{-16}	1/65536	-96.3	.000015	.0015	15

Table A Resolutions

"Useful Resolution," although typically not included in specifications, is a second type of resolution. Useful resolution is the smallest uniquely-distinguisable bit for all conditions of required operation (time, temperature, etc.) in other words, a 12-bit A/D may have only 10 bits of useful resolution from one extreme operating temperature to the other. Useful resolution is limited by "relative accuracy".

Accuracy, just as resolution, also has two distinctions. "Absolute Accuracy" defines the error of an A/D as caused by such things as gain error, nonlinearily, and noise. The error of an A/D converter at a given output code is the difference between the theoretical and actual analog voltage level required to produce that code. Since the code may be produced by any analog signal in a band of voltages the "required input voltage" is defined as the midpoint of the band of inputs. For example, if 5 volts (± 1.2mV) will theoretically produce a 12-bit half scale code of 100000000000, then a converter for which any voltage from 4.977 V to 4.999 V will produce that code has an absolute accuracy of 1/2 (4.997 + 4.999) - 5 volts = -2 mV.

Relative accuracy, expressed in %, ppm, or fractions of LSB, is the deviation of the analog value at any code (relative to the full analog range) from its theoretical value after the full-scale range has been calibrated. Since the discrete points on the theoretical transfer characteristic lie on a straight line, this deviation can also be interpreted as a measure of nonlinearity.

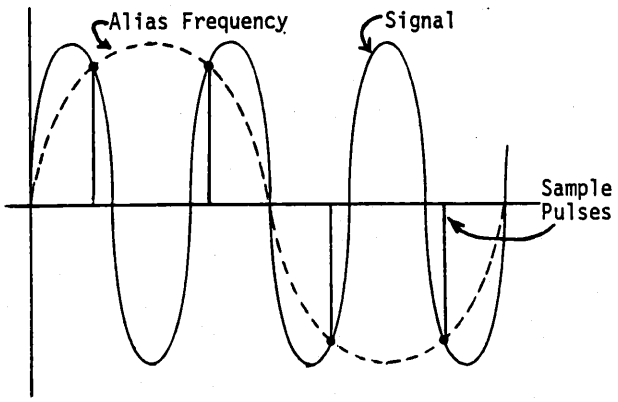


Figure 17

As can be seen, there are numerous technical factors to be considered when a digital relay is to be applied. If the signal conditioning subsystems are not properly designed and matched to the relay, the overall performance will be signficantly degraded.

CHAPTER III

ALGORITHMS FOR PROTECTIVE RELAYING

In the previous chapters, the reader has been introduced to the overall hardware configuration of a computer-based relay, as well as to some of the design specifics of the subsystem which samples the ac signals and enters them in digitized form into the processor memory.

In a conventional protective relay, the operating characteristics are completely defined in the design of the hardware. For example, the behavior of an electromechanical distance relay is dictated by transformers which modify the ac input signals, and by an induction cylinder unit which multiplies and integrates to yield a mho circle characteristic. This then defines the locus of apparent impedances for which the tripping contact will close. Computer relaying hardware is much more flexible, however, and can be used to monitor or control a variety of industrial processes. What makes it function as a specific power-system protective device is the software which digests the digitized samples of voltage and current waves into trip/no-trip decisions.

This Chapter takes an overview of the mathematical equations, or algorithms, which can be implemented in the processor to produce numerical quantities from sequences of data samples. These algorithm outputs form a basis for the relaying decision.

INTRODUCTION TO RELAYING ALGORITHMS

Assume for the moment that one wishes to perform simple overcurrent protection using a computer. That is, if the current magnitude exceeds some user-selected threshold, a trip output is to be initiated. At the input to the processor is a hardware subsystem, such as that characterized in Chapter II, which can sample, digitize, and store current-wave data in memory.

The problem may seem trivial, as it did to many of those who first seriously considered it in the late 1960's. The first proposed measurement schemes attempted to sample the current wave at its peak to obtain a value proportional to RMS magnitude [8]. The peak sample could be found either by detecting the zero-crossing and waiting 1/4 cycle (4.16 ms); or by detecting the zero crossing of the differentiated wave and sampling at that instant. The differentiated current wave leads the current wave by 1/4 cycle and can be obtained by looking at the secondary voltage of an unburdened air-gap or air-core transformer.

The peak measurement scheme had at least two recognized deficiencies:

1. In order to find the peak, the relaying processor required special interfacing hardware -- zero-crossing detectors and timing or differentiating devices in addition to the input elements mentioned in Chapter II.
2. Although rigorous performance-prediction procedures had not evolved at that time, it was obvious from inspection that any transient distortion present during the sampling would disrupt the measurement.

Relegating a sophisticated minicomputer to the comparison of a number with a limit while providing specialized external hardware seemed inappropriate and economically unattractive. The next obvious steps, then, were to attempt to move more of the processing burden into software while reducing the dependence of the accuracy on a single sample. This required signal-processing algorithms which did not need to be synchronized to the periodic waveforms being measured.

Asynchronous-Sample Algorithms

The bulk of this Chapter discusses the following categories of algorithms:

1. Sample-and-derivative calculations
2. Sinusoidal curve-fitting
3. Fourier-analysis and Walsh-analysis notch filtering.
4. Solution of differential equation of protected-system model.
5. Least-squares curve fitting.

This section introduces concepts which are common to all of them, starting with a detailed description of the first algorithm published for use with asynchronous data samples [19]. It belongs to category (1) above.

The equations below use the following symbols:

- i = Instantaneous value of the ac current waveform.
- i' = Instantaneous value of the derivative of the ac current waveform.
- i_k = The k^{th} instantaneous current sample value in an infinite sequence of such sample values.
- I_p = The peak value of the ac current sinusoid.
- ω = Angular frequency of the sinusoidal current wave in radians per second.
- t = Time instant relative to beginning of ac cycle, or relative to beginning of the measurement process.
- h = Fixed time interval between samples.

Consider a pure sinusoidal current of frequency ω:

$$i = I_p \sin \omega t \qquad (1)$$

The rate-of-change of this sinusoid at any instant is

$$i' = \omega I_p \cos \omega t \qquad (2)$$

One can see that when $i = 0$, i' assumes its maximum value; such a value is just a frequency-dependent constant times the peak of the original current. Therefore, the rate-of-change at the zero-crossing is a good indicator of peak value. Mann and Morrison [19] utilized the fact that a fixed computation using the sample value and the derivative yields the peak of the sinusoid regardless of where on the wave the sample is taken:

$$I_p = \sqrt{i^2 + \left(\frac{i'}{\omega}\right)^2} \qquad (3)$$

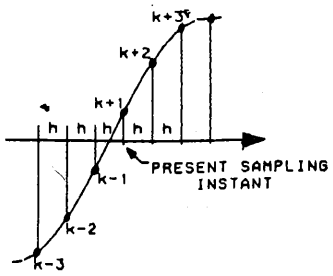


Figure 1. Asynchronous Sampling of Current Wave.

An expression for the phase position of the value on the sinusoid is:

$$\phi_i = \tan^{-1}\left(\frac{\omega i}{i'}\right) \qquad (4)$$

Peak and Phase Computations with Data Samples

The application of these expressions to relaying was a breakthrough, since it permitted the use of asychronous sampling, i.e., the sampling process did not have to be synchronized to the phase position of the sine wave being measured.

Consider asynchronous sampling of a current wave on a continuous basis with uniform time interval h between samples as shown in Figure 1. Sample number k is the present sample, while k-1, k-2, k-3, k-4 are the last sample, next older sample, etc. k+1, k+2, etc. represent "future" samples which are not yet available at the instant of time captured by Figure 1. We refer to the magnitude of the sampled current values as i_k, i_{k-1}, i_{k+1}, etc. Note that each time we take a new sample, we renumber all of the old ones -- i_k becomes i_{k-1}, i_{k-1} becomes i_{k-2}, and so on for all samples being considered.

We now wish to write equations (3) and (4) above in terms of these samples. Since a given sample value contains no infomation about the derivative at the sampling instant, the derivative must be approximated by computing a scaled difference including samples on either side of the sample point for which i' is needed. Figure 2 shows one possible way of doing this. The sampled data expression is

$$i_k' = \frac{i_{k+1} - i_{k-1}}{2h} \qquad (5)$$

Thus with asynchronous sample value i_k and the first-difference approximation to its derivative (5), we can compute I_p and ϕ_i.

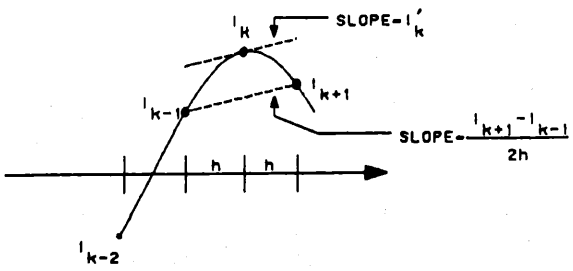


Figure 2. Example of Sample-Difference Approximation to Derivative.

Note that a total of three consecutive samples are needed. We say that this algorithm has a data window of 3 samples, or of 2h milliseconds. The next section reviews data windows.

Since the i_{k+1} sample was previously described as a "future" sample, the computations must be held up until i_{k+1} is available in a real system. Strictly speaking, we should always express the algorithm in terms of i_k, i_{k-1} and i_{k-2}. Nonetheless, in the literature algorithms are often expressed using samples like i_{k+1}, with the time delay needed in the implementation understood by the potential user.

Now consider the application of such an algorithm to a current wave whose peak magnitude increases suddenly due to a fault. Note that the instantaneous magnitude is constrained by power-system reactance from changing suddenly; this often gives rise to the decaying-exponential current transient associated with faults. Assume for now that the fault current is free of noise or harmonics and that the inception angle is adjusted to produce no decaying-exponential transient.

Also, assume that the input subsystem takes many samples for each ac period; for example 8 to 16 per cycle (i.e., h = 2.08 to 1.04 ms with f = 60 Hz). The relaying computer applies the algorithm recursively to the signal -- each time one new sample is taken, one old one is discarded and the calculation is repeated. Refer to Figure 3. The 3-sample data window is stepping along the wave, including new samples as they appear in the group of three used to compute I_p amd ϕ_i. For the prefault steady-state condition, each recursion yields the identical, correct values of I_p and ϕ_i.

Eventually the window reaches the fault inception point and the peak current magnitude suddenly becomes larger. At a time 3h units after the last prefault sample, 3 fault samples are available which the processor can use to calculate the fault-current magnitude. Keeping in mind that a noise- and transient-free fault signal was assumed, these three samples are sufficient to accurately compute the peak magnitude of the fault current, and thus to make the trip or no-trip decision. When the next fault-current sample is taken, the processor can repeat the computation, adding the new sample and discarding the oldest as before. The same peak magnitude number should be produced.

This provides a solution to the problem of relaying an ideal fault, but two key questions have been left unanswered so far:

(1) What algorithm results are produced during the transition interval when some of the samples are taken after fault inception and some remain from before inception. (i.e., when the data window includes the fault inception time as shown in Figure 3)?
(2) How well will the algorithm work when noise and transients are present in the signal?

Answering these two questions identifies the main tradeoffs one makes in selecting from the variety of available algorithms.

Data Window and Fault Inception

For the one algorithm considered so far, the computations performed when the window includes both prefault and postfault samples tend to yield poorly-defined intermediate results. While one might hope

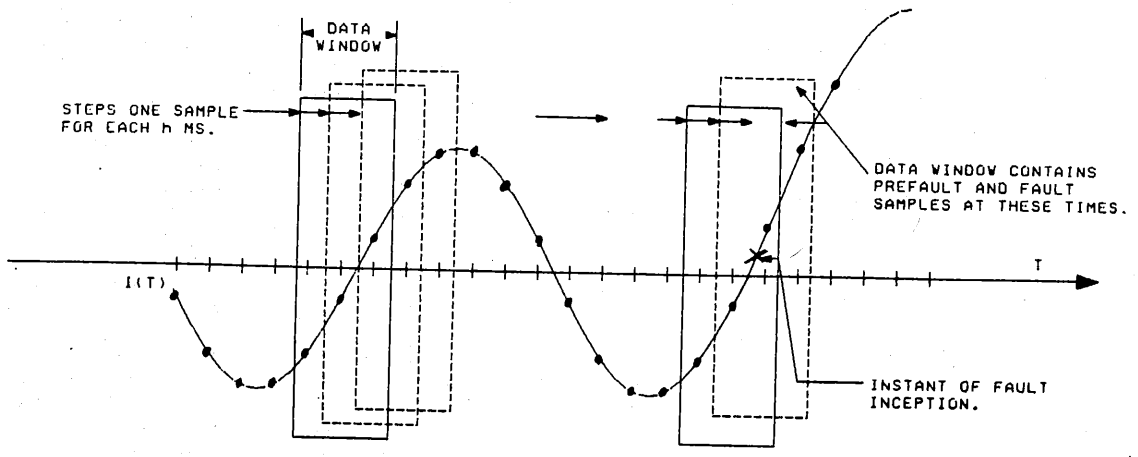


Figure 3. Data Window Stepping Along Current Wave.

for a smooth transition from prefault to fault peak values (and can obtain a smooth transition from some algorithms discussed later), this particular algorithm and many others yield unpredictable results while the window includes the moment of fault inception. Because of this,the processor must wait at least 3 samples after fault inception before it tries to establish the fixed fault current magnitude.

Effects of Noise and Transients

Of course, real fault waveforms are not pure as assumed so far. Depending on prefault load, fault inception angle and fault-current magnitude, a decaying exponential or dc-offset transient appears in the current with initial amplitude up to the peak of the fault current, and with a decay time constant of 30-50 ms for a typical EHV line. Nonlinear-impedance elements in the system, including the fault arc itself, may produce a number of harmonic components which are especially noticeable in the voltage signal. Other high-frequency noise may be present, including that associated with reflection of surge wavefronts between the bus and the fault , and that resulting from the eigenvalues of the faulted system. Finally, current transformers often saturate during faults, while capacitive-divider voltage transformers produce undesired subsidence transients. Consider how any algorithm, such as the Mann-Morrison algorithm used as an example so far, works when all of this distortion is present. Recall the assumed waveform from which that algorithm was derived - a pure 60 Hz sinusoid. With such a pure wave, only three samples are needed because the algorithm only requires enough data points to fit the sinusoid of the correct phase position and magnitude. If the samples are corrupted by other frequencies and nonsinusoidal signals, the wrong sinusoidal fit will be calculated. The size of the error depends on the magnitude of the undesired components. The next section looks at other algorithms which assume corrupted waveforms, and thus deal more effectively with them when they occur.

Performance Analysis Techniques

A transfer function, similar to that generated for continuous-time networks, can be used to analytically predict the behavior or response of an algorithm in the presence of distorted fault waveforms. This function can be found by using the z-transform, which resembles the Laplace transform with the jw-axis in the s-plane mapped into a unit circle about the origin of the z-plane. [40], Chapter 2 describes the z-transform. "Sampled-Data Control Systems" [J. R. Ragazzini and G. F. Franklin, McGraw-Hill Book Co., New York, 1958] also serves as an excellent tutorial reference on z-transforms. By transforming the algorithm into the complex-z domain and substituting frequency for the complex variable z (as we do to go from the Lalace to the Fourier transform) we can obtain a frequency response plot for the algorithm which is symmetric about the Nyquist frequency (one-half the sampling frequency) and which repeats after each integer multiple of the sampling frequency. This symmetry and repetition represents the folding or aliasing predicted by the sampling theorem as shown in Chapter II. We assume, as in Chapter II, that the input signal has been low-pass filtered with sufficient attenutation at the Nyquist or folding frequency so that we only need consider the algorithm response below this limit.

If we apply the z-transform to the Mann-Morrison algorithm and plot the frequency response, we obtain the result shown in Figure 4. To see the meaning of plot, consider the spectra of the power-system signals shown in Figure 5. (a) is an impulse at 60 Hz, representing magnitude of current the pure sinusoid before the fault occurs. Clearly, the multiplication of this magnitude by the 60 Hz algorithm response simply scales the amplitude; we already know that the scaling yields peak magnitude as an output. Next, consider the spectrum in 5(b). This shows an example of a fault signal, with a large 60 Hz component, a number of harmonics, a high-frequency traveling-wavefront component, and an exponential component produced by the decaying dc-offset transient. Only the high-frequency wavefront component is removed by the analog anti-aliasing filter; the rest of the distortion passes through the algorithm and affects the results. The multiplication of the spectrum and the frequency response function will yield a result showing the influence of all the components on the output. The frequency-response plot represents the average behavior of the algorithm over the full ensemble of possible phase relationships between a specific frequency components and the data window; individual realizations may show more or less response.

For the sampling rate shown in Figure 4 note that the algorithm is much more sensitive to some harmonics, notably the third harmonic, than it is to the desired fundamental. This illustrates the potential pitfalls of the optimistic assumptions on which the algorithm is based.

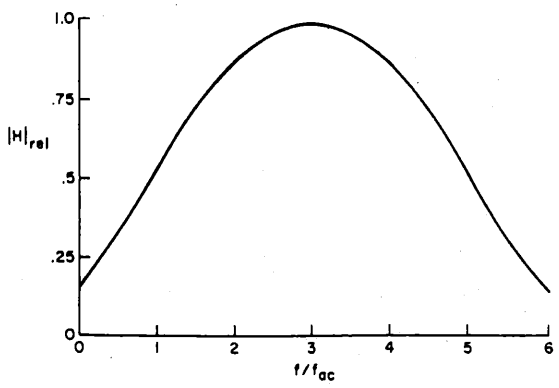


Figure 4. Frequency Response of Mann-Morrison Algorithm (12 samples per cycle).

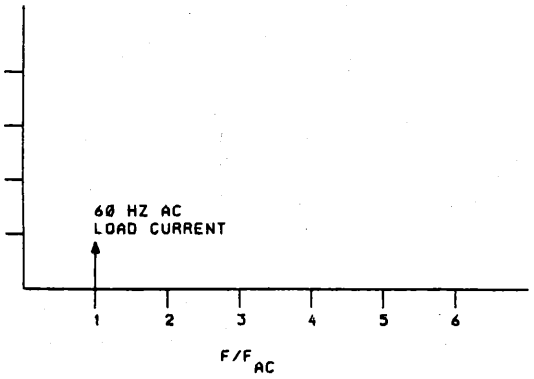


Figure 5. (a) Prefault Signal Spectrum Example.

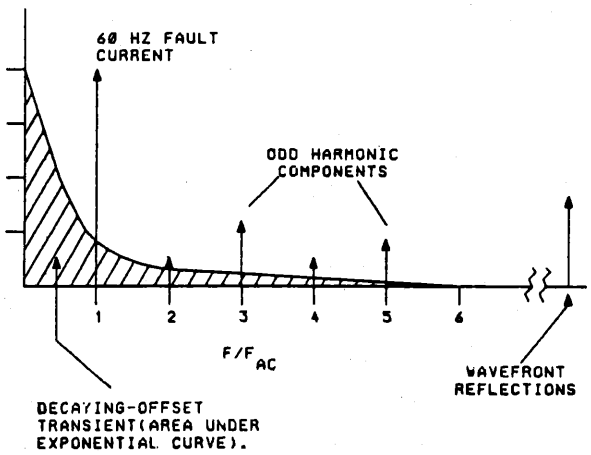


Figure 5. (b) Fault Signal Spectrum Example.

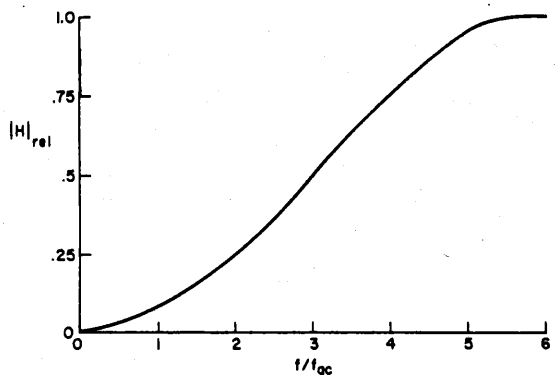


Figure 6. Frequency Response of Prodar 70 Algorithm (12 samples per cycle).

For distortion above the fundamental freuqency, Mann and Morrison proposed in [19] a digital-filtering calculation which averaged samples over a short time span to attenutate the undesired components. Also, they recognized the harmful effects of decaying-dc offset transients on their algorithm and proposed the use of a mimic-burden -- an R-L series network whose time constant matches that of the protected power network. Connecting this burden in parallel with the current input to the relaying computer suppresses offsets of the assumed time constant.

Errors resulting from fault-waveform distortion point to the desireability of finding an algorithm which is highly frequency-selective -- one which has a sharp response peak at 60 Hz and little or no response elsewhere. So long as the specified frequency-response is consistent with criteria of casuality for filters we can design a practical implementation. However, a basic principle of communications theory states that a signal cannot be strictly bandlimited and strictly timelimited simultaneously; constriction of either time or bandwidth entails expansion of the other. In terms of algorithms, we therefore predict that to filter the input data we must take samples for a longer time interval then for the Mann-Morrison algorithm; i.e., we will need a long data window. As a consequence, we will have to wait a long time after fault inception to accumulate enough data for a post-fault steady-state measurement. The fulfillment of this prediction is found in the discussion of additional algorithms in the next section.

Distance Relaying on a Computer

Subsequent chapters present specific techniques for line, bus, generator, and transformer protection; the goal here is only to provide a basis for understanding how computations of steady-state magnitudes and phase positions are executed regardless of application. However, this subsection introduces the notion of line protection by distance measurement since some of the algorithms which are of general interest have been formulated for this purpose. Also, line protection serves as a basis for examples in the section on performance tradeoffs below.

Protection of an important transmission line is most frequently performed using phase- and ground-distance relaying techniques. In a computer-relaying system for a transmission line the goal is then to extract the apparent impedance from the line terminal to the fault from the data samples.

With the example algorithm above, one obtains apparent impedance by calculating the peak voltage magnitude and phase position, and the peak current magnitude and phase position. Then, the computer executes a complex phasor division to calculate apparent impedance. The result is produced in polar form $Z < \theta$, but can be readily converted to or directly computed in rectangular form $R + jX$ if desired. In general, it is possible to obtain the results in either form directly, or by converting from one to the other. Specifically, some of the algorithms discussed below use both voltage and current signals as inputs, and directly yield complex phasor impedance in rectangular form without the intermediate computation of voltage and current magnitudes and phases.

Details of the line protection problem will be discussed in Chapters IV and V.

ADDITIONAL ALGORITHMS

This section provides only a sample showing the range of available algorithms. The list at the end of this chapter cites a number of references in the Bibliography, Chapter IX, which include additional algorithms.

1. Prodar 70 Algorithm

In 1971, a computer based transmission-line relaying system designed by Westinghouse [24,25] was placed in experimental service at a Pacific Gas and Electric Co. substation as part of a joint project described in Chapter IV. The designers were concerned in this case with two types of distortion of the sinusoidal relaying signals -- dc-offset transients, and subnormal frequency components caused by nearby series-capacitor banks during faults. Accordingly, they took the Mann-Morrison algorithm described above and modified it to use first and second differences, rather than raw sample values and first differences. This aproach leads to equations 6 and 7 for the peak and phase values.

$$I_p = i'^2_k + \left(\frac{i''_k}{\omega}\right)^2 \qquad (6)$$

$$\theta_i = -\tan^{-1}\left(\frac{\omega i'}{i''}\right) \qquad (7)$$

where

$$i' = \frac{1}{2h}(i_{k+1} - i_{k-1}) \qquad (8)$$

is the first-difference approximation as before and

$$i''_k = \frac{1}{h^2}(i_{k+1} - 2i_k + i_{k-1}) \qquad (9)$$

is the second-difference approximation to the second derivative. The extra differentiation reduces the sensitivity to dc-offsets, subnormal signals, and all other distortion of frequency below the power-system fundamental. However, it also accentuates the errors from harmonics and high-frequency distortion, so that post-algorithm integration must be used to obtain usefully stable results. Compare the frequency response in Figure 6 with that in Figure 4. Observe how the extra differentiation has heavily skewed the response towards higher frequencies. This has not, however, substantially altered the overall selectively, which is still limited by the three-sample window.

2. Sinusoidal Curve Fit

This algorithm, developed by Pennsylvania Power and Light Co. [51], uses voltage and current samples to directly calculate apparent resistance and reactance to the fault. The computation is based on fitting data to fundamental sinusoidal quantities (voltage and current) using three consecutive samples. Equations for X_L and R are

$$X_L = \frac{v_{k-1}i_k - v_k i_{k-1}}{(i^2_{k-1} - i_{k-2}i_k)\csc\Delta} \qquad (10)$$

$$R = \frac{2v_{k-1}i_{k-1} - v_k i_{k-1} - v_{k-2}i_n}{2(i^2_{n-1} - i_{n-2}i_n)} \qquad (11)$$

where $\Delta = 2\pi hf$ is the constant angular displacement between samples (in radians).

The equations respond rapidly to changes in the incoming data, but are susceptible to high-frequency transients. Note the sensitivity to the third harmonic in the frequency-response plot of Figure 7.

3. Full-cycle Fourier Algorithm

Ramamoorty [28] was the first of many to propose that the desired fundamental voltage or current be extacted from the fault transients by correlating one cycle of data samples with the stored samples of reference fundamental sine and cosine waves. Figure 8 illustrates the process.

Note that waveform description is initially produced in rectangular form. The general expressions for the sine and cosine components of voltage at a sample point k are

$$V_s = \frac{1}{N}\left[2\sum_{\ell=1}^{N-1} v_{k-N+\ell}\sin\left(\frac{2\pi}{N}\ell\right)\right] \qquad (12)$$

$$V_c = \frac{1}{N}\left[v_{k-N} + v_k + 2\sum_{\ell=1}^{N-1} v_{k-N+\ell}\cos\left(\frac{2\pi}{N}\ell\right)\right] \qquad (13)$$

where the v_i are the voltage samples and N is the number of samples taken per fundamental cycle. Similar expressions are evaluated for current components I_s and I_c. These may be converted to polar form using

$$V = \sqrt{V_s^2 + V_c^2} \qquad (14)$$

$$\phi_v = \tan^{-1}\left(\frac{V_s}{V_c}\right) \qquad (15)$$

Implicit in Fourier analysis is drastic filtering of the data; the output responds slowly, smoothly, and accurately to badly distorted fault waveforms.

The frequency response plot of Figure 9 shows the response peak to the power system frequency, with nulls at dc and at each harmonic. High frequencies above the second harmonic are all well attenuated.

The minor lobes of response between the harmonics are referred to as leakage and result from the finite time window. The minor peaks can be attenuated by pre-weighting the samples before algorithm processing, at the expense of loss of the main-lobe resolution. This is shown in a subsequent section of this Chapter.

The Fourier method can be extended to use multiple cycles of data, if relaying time permits. The filtering becomes even sharper, and the response slower.

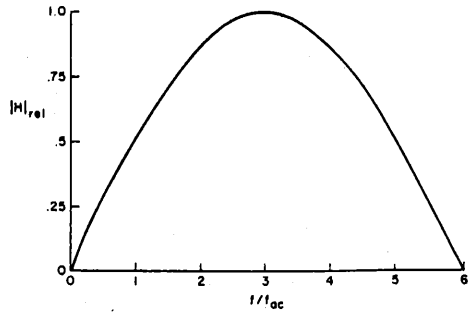


Figure 7. Frequency Response of Sinusoidal Curve Fit Algorithm (12 samples per cycle).

This algorithm yields the best filtering of any algorithm discussed here; or, in fact, of any algorithm using this size data window. Recall our prediction that the algorithm with well-bandlimited response collects data for a long time - this one takes a full cycle to converge on the post-fault stead-state result, as the long window steps from prefault to postfault data.

4. Fourier Algorithm with Shortened Window

A highly effective compromise between speed of response and sharpness of filtering has been struck by Phadke et al [62]. The basis for this method is the same as for the full-cycle Fourier method, but the data window is shortened to 1/2 cycle plus one sample for faster response:

$$V_s = \frac{4}{N} \sum_{\ell=1}^{N/2} v_{k-(N/2)+\ell} \sin\left(\frac{2\pi}{N}\ell\right) \qquad (16)$$

$$V_c = \frac{4}{N} \sum_{\ell=1}^{N/2} v_{k-(N/2)+\ell} \cos\left(\frac{2\pi}{N}\ell\right) . \qquad (17)$$

Of course, accuracy of results is more seriously affected by off-normal frequency components; dc offsets present a particular problem. The authors of the algorithm remedy the latter by assuming that the fault waveform contains a dc offset of unknown magnitude but with time constant determined by the known X/R ratio of the line. The suggested implementation effectively finds the magnitude of the offset and subtracts it from the fault waveform prior to the Fourier analysis itself.

The response plot of Figure 10, when compared to that for the full cycle Fourier algorithm, shows slightly reduced effectiveness in coping with dc and even harmonics as expected. This is overcome, in part, by the dc offset correction.

5. Walsh-Function Algorithm

The Walsh Function algorithm [53] is closely related to the Fourier algorithm of 3 above. The orthogonal functions which are correlated with the fault waveform, however, are not fundamental sine and cosine functions, but Walsh functions — a fundamental pair of odd and even square waves, plus a set of harmonically-related square waves whose transitions occur according to a binary-counting sequence.

Real-time computation is simplified since the reference square waves assume values of ± 1 only. However, this benefit may be mitigated in some applications by the need to extract several harmonics of the square-wave components along with the fundamental so that the desired fundamental sinusoidal component can be reconstructed from the Walsh functions.

As for the full-cycle Fourier algorithm, the filtering of the source data is drastic, and the resultant output is thus heavily damped. Accuracy is good even for distorted waveforms.

Note that the frequency response plot of Figure 11 is given for a sampling rate of eight per cycle, rather than 12 as in the other cases; the Nyquist limit coincides the with the fourth harmonic. This is because the Walsh method is convenient to implement only for a number of samples which is an integral power of two. Although this plot is not directly comparable with the Fourier plot above, the two algorithms, in fact, behave almost identically if implemented for the same sampling rate.

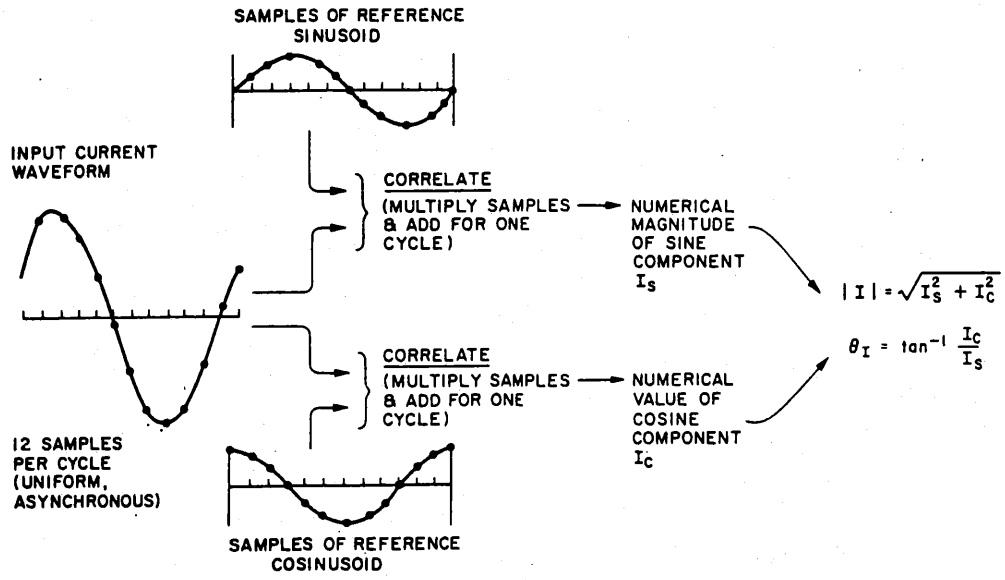


Figure 8. Fourier Notch-Filter Algorithm.

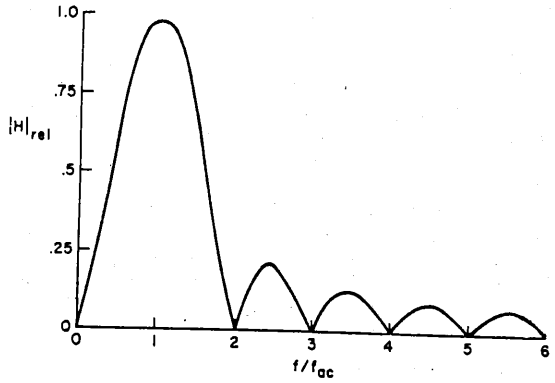


Figure 9. Frequency Response of Full-Cycle Fourier Algorithm (12 samples per cycle).

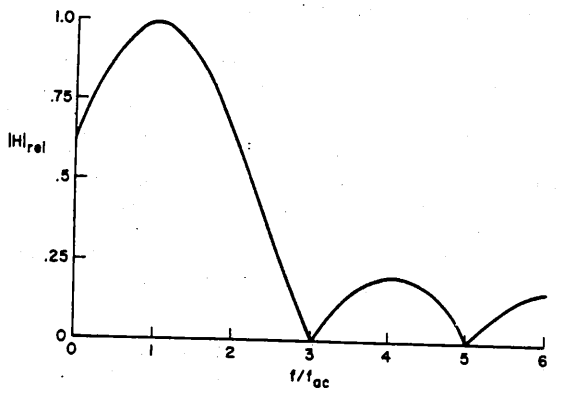


Figure 10. Frequency Response of Fourier Algorithm with Shortened Data Window (12 samples per cycle).

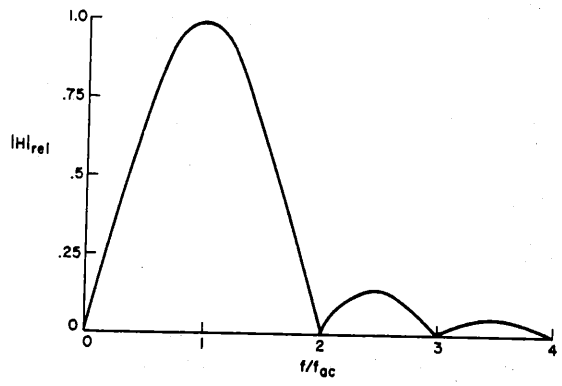


Figure 11. Frequency Response of Walsh-Function Algorithm (8 samples per cycle).

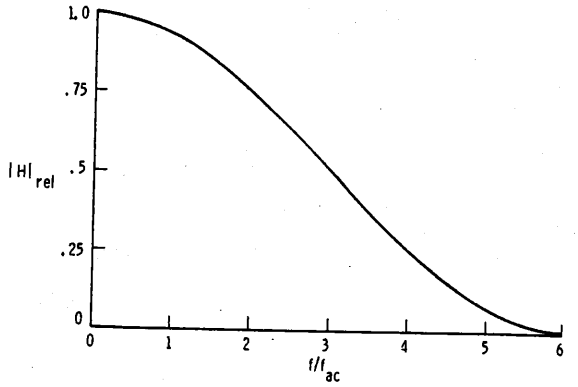


Figure 12. Frequency Response of Differential-Equation Algorithm (12 samples per cycle).

6. Differential-Equation Algorithm

Taking an ingeniously different view of the problem of apparent-impedance measurement for a transmission line, McInnes and Morrison [16] proposed that the line being protected be modeled as a series R-L circuit resulting in the following equation:

$$V = R_{eff} i + L_{eff} \frac{di}{dt} . \qquad (18)$$

Solution for the R and L parameters is accomplished by integration over two successive time periods and solution of the resulting simultaneous linear equations. Integrations are performed using the trapezoidal rule. The sampled-data expressions are:

$$L = \frac{h}{2} \frac{(v_{k-1}+v_{k-2})(i_{k-1}+i_k)-(v_{k-1}+v_k)(i_{k-1}+i_{k-2})}{(i_{k-1}+i_k)(i_{k-1}-i_{k-2})-(i_{k-1}+i_{k-2})(i_k-i_{K-1})} \qquad (19)$$

$$R = \frac{(v_{k-1}+v_k)(i_{k-1}-i_{k-2})-(v_{k-1}+v_{k-2})(i_k-i_{k-1})}{(i_{k-1}+i_k)(i_{k-1}-i_{k-2})-(i_{k-1}+i_{k-2})(i_k-i_{k-1})} \qquad (20)$$

This algorithm has the advantage of recognizing dc offsets as valid components of fault currents rather than processing them as unexpected transients — such offsets are predicted by the lumped R-L model on which it is based. This model is valid for lines that are not extremely long, permitting shunt capacitance to be neglected. For long lines, shunt-admittance effects introduce some error but do not corrupt the results excessively, in general.

One recent work [88] has attempted to develop an algorithm from a model which includes lumped admittance elements, but the computational burden on the computer increases severely.

The plot of Figure 12 is for a data window of 5 samples, which is one of the many possible windows for which this algorithm can be implemented (down to 3, as in (19 and (20) above). High-frequency response falls off to a null at the Nyquist limit. The large response to dc and low frequencies does not reflect unfavorably on the ability of the algorithm to deal with the exponentially decaying dc offset whose occurrence is consistent with the line model.

A highly-effective algorithm related to the one just given was developed for an experimental computer relaying system developed by the General Electric Co. [66,85]; this project is described in detail in Chapter IV.

Ranjbar and Cory [49] have proposed a related algorithm in which the limits of integration have been selected to introduce nulls at particular harmonic frequencies. The method is very effective in this regard, but does have a generally longer data window. Also, it tends to ring on fault inception so that the results oscillate severely until the window is completely filled with fault data.

7. Least-Squares Fitting Algorithm

The Fourier algorithm can be shown to be a means of fitting a fundamental sinusoid to the fault-data samples with the minimum possible mean-square error. More sophisticated algorithms have been proposed which perform a similar fit, but to a sinusoid having an exponentially-decaying dc transient and/or harmonic distortion.

Luckett et al [47] claimed to have performed a least-squares fit to the general fault waveform:

$$K_1 e^{-\lambda t} + \sum_{m=1}^{N} (K_{2m} \sin m\omega t + K_{2m+1} \cos m\omega t) \qquad (21)$$

where the solution for the K values is found by a least-squares fit of the form which minimizes the mean-square error between the assumed and actual waveforms. Few details regarding the implementation of the algorithm are given in [47]; many such fits are possible. Figure 13 shows the frequency response for a least-squares algorithm using a 10-sample window with 12 samples taken per ac cycle. In all of these, a decay time constant $1/\lambda$ for the offset transient is assumed.

In a more recent and complete presentation, Sachdev and Baribeau [92] suggest a least-squares fitting algorithm which solves simultaneous equations to obtain parameters of the fault waveform from a series of voltage or current samples. Seven parameters describing a fundamental component, a dc-offest transient whose decay time constant need not be assumed, and a third harmonic component, are identified. If seven samples are used, the equations can be expressed in matrix form as

$$[A]\ [x] = [v] \qquad (22)$$

where [x] is the desired parameter vector, [v] is the sample vector, and [A] is a square matrix of constants. Multiplying both sides on the left by $[A]^{-1}$ solves the system for [x].

Accuracy can be improved by expanding the data window; i.e., by increasing the size of [V]. If this is done, [A] is no longer square and cannot be inverted. However, we can apply the well-known method of least-squares as expressed in matrix form:

$$[A]^T[A]\ [x] = [A]^T[v]. \qquad (23)$$

[x] and $[A]^T[v]$ do have the same number of elements, and $[A]^T[A]$ is square, so that this system can be solved as before. The resulting parameter-set [x] describes the waveform which fits the data points [v] with minimum mean-square error.

The computations are minimized by finding only the two fundamental-wave parameters in [x]. Also, many of the computations in (22) can be performed a priori and incorporated in the program. The authors of [92] describe how they optimize sampling rate and data-window size.

PERFORMANCE TRADEOFFS

The following figures graphically illustrate the strengths and weaknesses of algorithms having different frequency-response characteristics. They have been extracted from a study effort of Westinghouse and Pennsylvania Power and Light Co., a portion of which is described in [70]; they are among thousands of tests executed on a variety of algorithms using simulated and actual fault data.

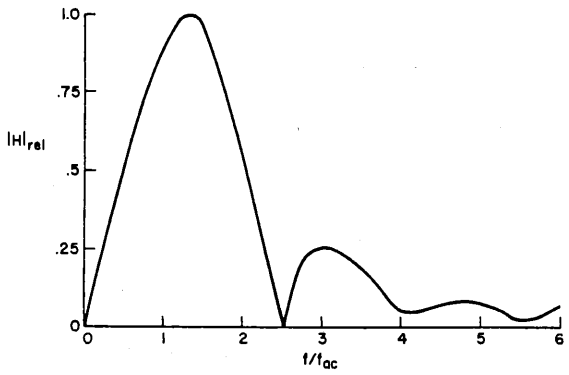


Figure 13. Frequency Response of Least-Squares Fitting Algorithm (12 samples per cycle).

Figure 14 shows the response of the full-cycle Fourier algorithm to a simulated transmission-line fault which is free of distortion, except that the inception angle has been adjusted to produce a full offset transient of 30 ms time constant in the current signal. The algorithm is used to calculate voltage and current magnitude, each in rectangular form; the apparent impedance to the fault in rectangular form, R + jX, is calculated from these, and R and X are plotted in Figure 14 as independent functions of time. The figure shows results for a sampling rate of 32 per cycle, which is higher than would probably be used in an actual mini- or microcomputer application but gives a clearer display of the results. The X component of apparent impedance is shown by the larger astericks; the smaller dots represent calculated values of resistance. The first result on the left is that calculated for the last prefault sample; the plot shows the drop in calculated impedance as the algorithm data window moves into the fault. The plotting continues for two cycles after the fault inception time.

As expected, the one-cycle window (32 samples in this example) of the Fourier algorithm results in a slow, gradual response to the fault. The variation in X during the second cycle, when the window is completely filled with fault data, is due to the effect of the decaying offset, but has been accentuated slightly by the resoltuion limitation of printer plotting used here.

Although the example shows complex impedance results, analagous behavior is obtained for current-only or voltage-only computations. In the current-only case, one would see the calculated magnitude rise gradually from the prefault to the fault value, with some slight variation after the first cycle due to the offset.

Figures 15 through 18 show results for other algorithms and faults, as simple examples of the performance tradeoffs explained earlier. In Figure 15 the Mann-Morrison algorithm with a window of only three samples and a digital version of the dc-offset mimic-burden filter processes the same fault as was used in Figure 14. Not surprisingly, the Mann-Morrison method produces almost perfectly accurate results starting four samples after fault inception, while in the Fourier analysis case the results do not stabilize near the expected values until the full one-cycle (32-sample) data window moves into the post-fault interval. Using this fault alone for comparison, one would question why the Fourier algorithm would be considered for any relaying application.

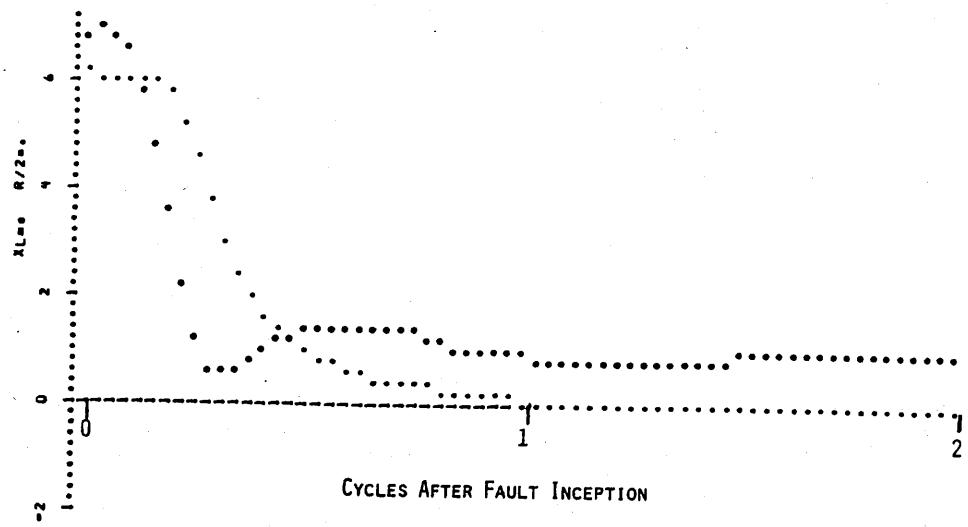


Figure 14. Response of Fourier Line-Protection Algorithm to Fault with Full Offset in Current.

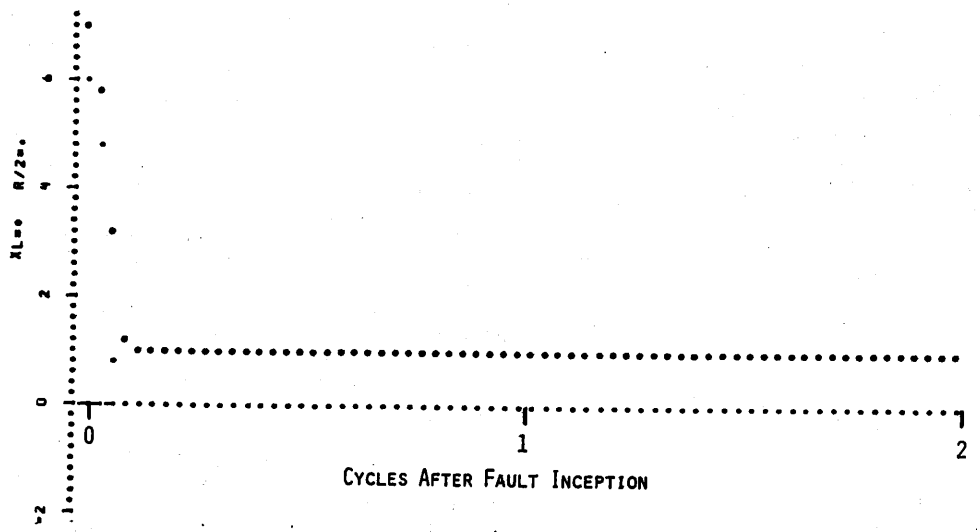


Figure 15. Response of Mann-Morrison Line-Protection Algorithm to Fault with Full Offset in Current.

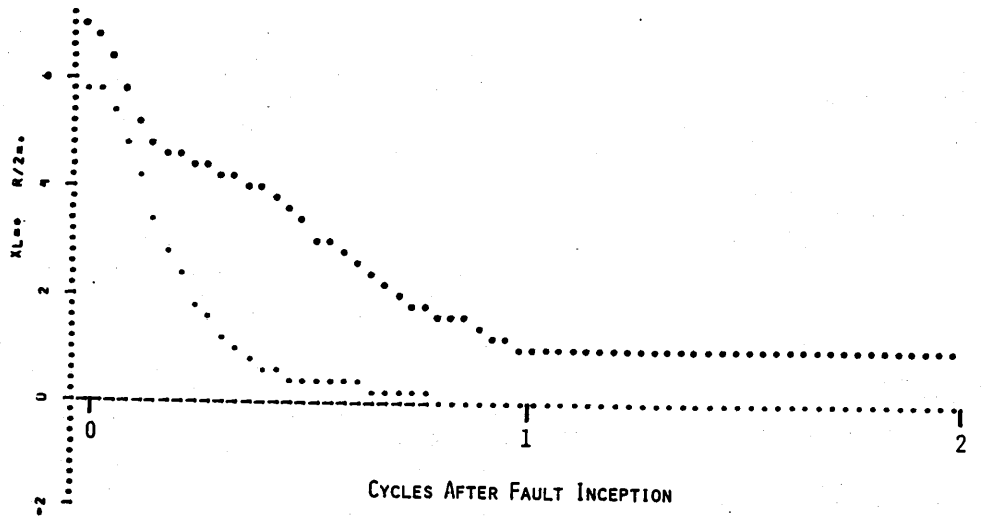


Figure 16. Response of Fourier Line-Protection Algorithm to Fault with Harmonics in Voltage.

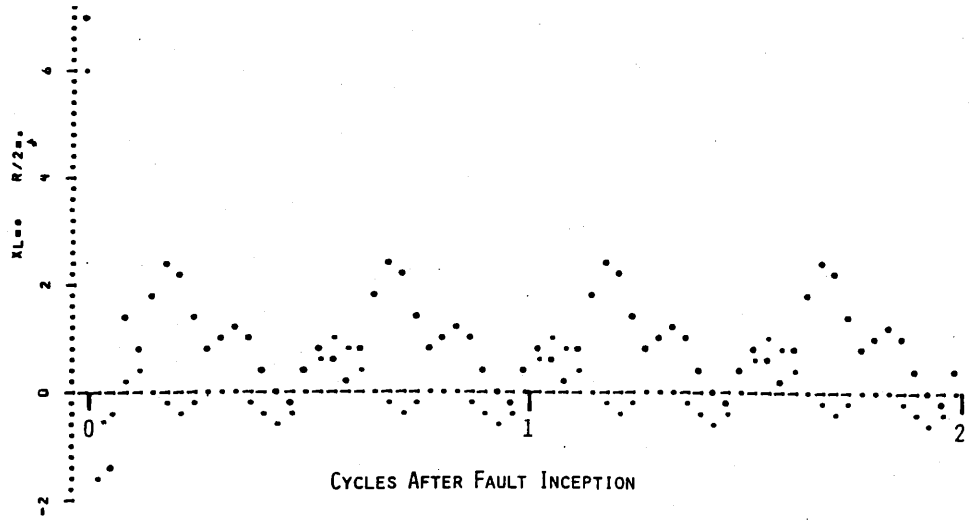


Figure 17. Response of Mann-Morrison Line-Protection Algorithm to Fault with Harmonics in Voltage.

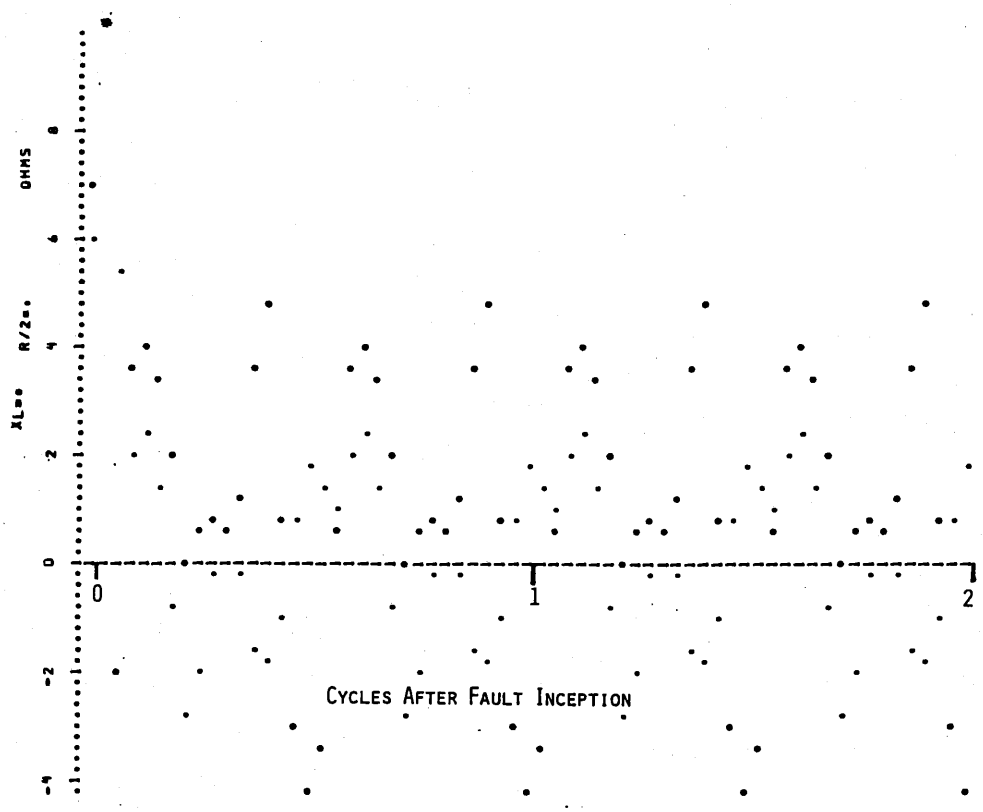


Figure 18. Response of Prodar 70 Line-Protection Algorithm to Fault with Severe Harmonics in Voltage.

To answer this point, study Figures 16 and 17. The offset in the test current has been removed by adjustment of fault inception angle, and the voltage wave has been contaminated by harmonics. Third and fifth harmonics, having no decrement, are added with magnitudes of 15% and 7.5%, respectively, of the prefault voltage (they constitute larger percentages of the collapsed fault voltage).

The Fourier algorithm, demonstrating its filtering ability, still converges slowly and steadily on the expected values, yielding very low errors after one cycle. The broadbanded Mann-Morrison algorithm, on the other hand, shows the harmonic content in its output and provides highly variable, marginally useful results.

Finally, Figure 18 shows the response of the Prodar 70 algorithm (whose frequency-response plot shows a tendency to severely accentuate high frequencies) to a fault with the same harmonic content. Obviously, such flypaper-like results are useless as they stand and additional processing must be added.

In virtually all cases, as in the examples just given, the performance traits predicted by analysis are confirmed by testing with real or simulated fault data.

A fact which sheds encouraging light on the entire matter of algorithm performance is that one of the more harmonic-susceptible algorithms, the Prodar 70 computation, has performed securely and effectively in nearly eight years of field service. Newer algorithms can only yield better results.

EXTERNAL MODIFICATION OF ALGORITHM RESPONSE

Most of the above discussion has implied that the algorithmic computation itself should have all of the desired signal-processing capabilities needed for relaying built in. Whie this is probably beneficial from the computational-burden point of view, it is not the only approach to the problem. Another sensible technique is to use a less-than-optimum algorithm (perhaps a computationally-simple one), and then to improve its characteristics by applying specific preprocessing and postprocessing remedies. The following four categories should be considered by the designer of a digital relaying system.

1. Analog Prefiltering

In Chapter II it was explained that an analog filter is inserted ahead of the sampling device to prevent aliasing problems. Since this filter must always be used, it may be possible to adjust the component values so as to provide some needed high-frequency attenuation at little or no cost. In fact, a filter which does not introduce severe phase delay at 60 Hz must roll off somewhat gradually, so in fact the user should consider the effect of this on overall response to harmonics whether or not additional harmonic attenuation is sought.

2. Digital Prefiltering

Once the data samples are brought into the processor, techniques can be borrowed directly from the theory of digital filtering to weight the spectrum in virtually any desired way. The tradeoffs of such techniques, in general, are the same as those we saw for the algorithms themselves -- sharp filtering entails a long string of data samples and slow response to sudden changes of the filter input.

As a case in point, the authors of [41] have designed a microprocessor-based distance relay in which sharp filtering is provided by a digital filtering program. This filtering removes most transients, so that a very broadband, 2-sample window algorithm can follow it. Despite the speed and distortion sensitivity of the basic algorithm, the response of the filter-algorithm cascade is accurate and damped like that of the Fourier method. Also note that Mann and Morrison [19] suggested digital prefiltering for their short-window algorithm.

If the user wants to suppress particular distortion frequencies or frequency bands to which the algorithm is sensitive, he can draw from design principles for digital filters as described in a broad range of texts such as [40]. Unfortunately, however, all but the simplest of these digital filtering methods require more computation than a microcomputer or microprocessor can handle in the time available between sampling instants, considering the number of ac quantities involved and the total bulk of the relaying programs which must be executed in the same time frame. [41] and [19] give examples of filters which are practical for real-time computation.

A specific preprocessing operation aimed at current-measuring applications for relaying is the removal of dc offsets. Mann and Morrison suggested an analog mimic-burden mentioned above; such a scheme can also be implemented in processor software. Phadke et al [62] describe one particular digital offset-removal computation. All such methods assume a time constant or X/R ratio; the cancellation of the offset is only partial if source or fault resistance effects modify the offset time constatnt. Incidentially, this is also true for the differential-equation algorithm.

3. Post-Processing of Results

Once a string of output values is produced by the algorithm, the relay engineer is faced with the need to reduce them to a trip or no-trip decision. The way in which this is done can modify the apparent behavior of the algorithm substantially.

A number of such post-processing methods and decision criteria have been published. The Prodar 70 experimental line-protection system[24] integrates the results and compares them with line-protection zone limits in a single operation which suppresses inappropriate noise-induced trips, and yields an inverse time-distance characteristic. In general, numerical integration is the most appropriate means of obtaining an inverse time-magnitude tripping characteristic for any measurement.

Gilbert and Shovlin [51] have suggested a tripping criterion in which one checks to be sure that the measured quantity exceeds the operating threshold; also, the calculated numeric values must be consistent to within a 12.5% band for three consectutive calculations. The latter test helps to insure that, for a short-window algorithm, the results are not being wildly perturbed by harmonics or other distortion. If they are, the program continues to compute measurements but will not trip until the noise subsides and the output stabilizes. The General Electric-Philadelphia Electric experimental relaying project [66] described in Chapter IV successfully uses a similar criterion.

For long-window algorithms, or for an algorithm used with a long-window digital prefilter, the user need not worry so much about disruption of results by transients. A simpler decision criterion, such as a simple trip-above-threshold check for two samples can be safely used in many applications. Note that the algorithm results always change smoothly as the window moves into the fault -- if the post-fault steady-state magnitude is well above the threshold, the locus of computed values in a plot like Figure 13 will cross the decision threshold well before the window is filled with post-fault data. We can be sure that the results will not swing back outside the threshold as it might for some short-window algorithm, so we can initiate a fault trip decision in much less than one cycle for these cases.

In summary, the post-algorithm processing should be tailored to the algorithm response and the

application. The user's ingenuity plays a key role in its development.

4. Data-Window Weighting Functions

The very act of selecting the number of samples to be included in a data window has a frequency-response or transfer function associated with it. This explains, in part, why there is high correlation between window size and filtering sharpness of any algorithmic computation. All of the algorithms characterized here use rectangular windows, which is the same as saying that all the samples in the algorithm window are supplied to the algorithm without modification.

It is also possible to weight or scale the samples according to some preselected function; each sample is weighted according to its relative position in the window (this means that the weighted sample values must be recomputed each time a new sample is available, before algorithm processing). Figure 19(a) shows the Hanning or raised-cosine window which is sometimes used in connection with the discrete Fourier tranform. The dots on the curve show the weighting factors which would be applied to 12 samples lying in a one-cycle data window.

Such weighting functions tend to smooth out the frequency-domain extremes in the transfer function of the algorithm which follows. For example, it can be used to trade main-lobe resolution in the Fourier algorithm response for reduction of the leakage peaks between harmonic frequencies. This is shown in Figure 19(b). The solid curve shows the frequency response associated with a one-cycle rectangular data window (obtained by taking a Fourier transform of the window). For comparison, the dotted curve shows the transform of the Hanning window. Note how the first null in the former is lost in the latter; but the sidelobe response is greatly attenuated beyond the second null for the Hanning window.

The relay-oriented user should beware of the effect on dc-offset response. If the Hanning window of one cycle duration is used in cascade with the Fourier notch-filter algorithm, the dc null of the algorithm itself is lost. The cascade frequency-response has a normalized value of 0.5 at dc. The dc null can be regained only by extending both the Hanning window, and the Fourier algorithm itself, to 2 cycles.

There are a number of such weighting functions, having differing degrees of effect, described in the literature on digital filters and the discrete Fourier transform. Cascading a window function adds considerable processing burden to obtain a rather subtle change in the results, so relaying application is limited to slow protection functions, and special implementations.

SELECTION OF ALGORITHMS

There is no single algorithm which is universally optimum. To select one, the potential user must consider:

1. Available Processor Capability

Implementing even the simplest of the algorithms in real time on a small computer to protect some element of a power system can present quite a programming challenge. The computations, involving varying degrees of multiplication and division, must

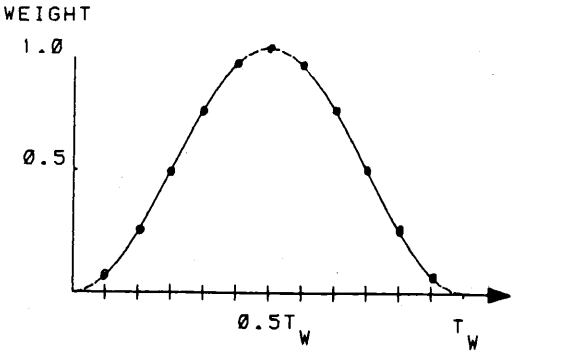
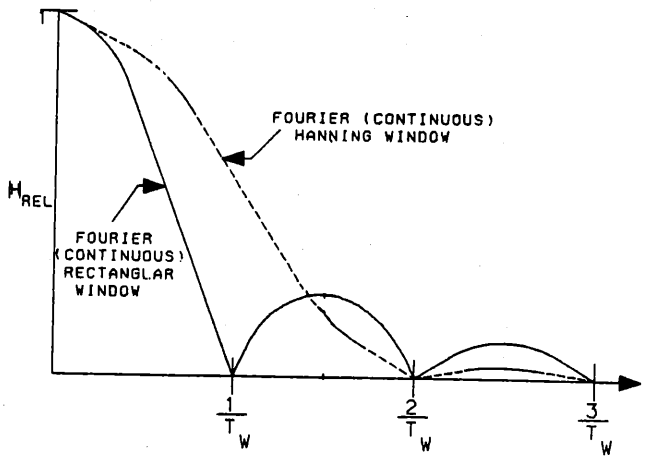


Figure 19. (a) Hanning Window Weighting Function.



(b) Fourier Transforms of Rectangular and Hanning Window Weighting Functions.

be repeated for every new sample and possibly for each phase. Unless an uneconomically large computer is available, relaying speed and algorithm sophistication are severely limited by processor capability. Therefore, choosing the fastest processor in a given category is a critical first step. Then, one must simulate or test prospective algorithms to find out which ones the processor can handle.

Popular 8-bit microprocessors which lack multiply or divide hardware impose the most severe restrictions on algorithms for complex relaying applications. [54] and [72] are intriguing examples of how moderately-fast relaying algorithms have been developed for real-time application on small computers, using few or no multiplications or divisions. These schemes use Fourier or Walsh analysis with sampling rate adjusted so that multiplications involve ± 1 only.

2. Speed - Accuracy Tradeoff

Ignoring processor-speed limitations, relaying speed may be traded for effective accuracy of the decision boundary. By clever design of post-algorithm processing, the tradeoff can be virtually optimized for each fault individually; this yields the inverse time-magnitude characteristic.

3. Adequate Filtering

The filtering ability of the algorithm and any preprocessing must be based on the expected transients in the relaying signal.

4. Speed - Sampling Rate Tradeoff

For a given algorithm, relaying speed can be sacrificed to lessen computational burden on the processor, by reducing sampling rate and modifying the algorithm accordingly. Keep in mind that sampling slower than 4 times per cycle begins to degrade the fundamental quantity whose changes are measured to perform the relaying. At the other extreme, sampling faster than about 16 times per cycle yields diminishing returns of speed, due to limits in the basic fundamental-frequency information content of a group of samples taken so close together.

Reference [70] describes a specific testing and evaluation procedure involving a number of algorithms. The results are not reported here since they are totally dependent on the criteria of performance which were of concern to those investigators. The procedure described there, however, should be regarded as a means of uniformly comparing algorithms according to any appropriate criteria the reader feels are important in his application.

SUMMARY

This Chapter has provided an overview of signal-processing methods used to make relaying decisions from data samples. The basic terminology of relaying algorithms has been developed, and means of analyzing and predicting performance have been presented. A representative selection of specific algorithms has been given along with the fundamental performance characteristics of each. Modification of algorithm response by pre- and post-processing has been reviewed. Finally, criteria to be used in selecting algorithms have been discussed.

The following list of reference numbers will guide the reader to those papers in the Bibliography, Chapter IX, which contain specific algorithms of the type described in this Chapter. In spite of the large number of implementations, one must recognize that many of the methods are closely related to one another. The references are [16], [19], [24], [26], [28], [34], [35], [38], [41], [47], [48], [49], [51], [53], [54], [58], [60], [62], [66], [69], [70], [71], [72], [81], [86], [87], [88], [89], [94].

CHAPTER IV

LINE RELAYING I

Three examples of digital relay systems for the protection of transmission lines are presented. The three systems are the Pacific Gas & Electric - Westinghouse PRODAC-70 project, the General Electric - Philadelphia Electric Co. digital relay project, and the American Electric Power Corp. digital relaying system. The PRODAC-70 project used a single terminal, while the GE/PE project had terminals at each end of the line. The AEP system uses one terminal but will communicate with equipment at the other end of the line. All three systems have had field tests although the latest AEP system is scheduled for field tests in 1979. Descriptions of each system as well as discussion of results both in the laboratory and the field are included.

BACKGROUND

Descriptions of the various aspects of computer relaying have been given in the previous presentations of the functional blocks, signal conditioning, and various algorithms. The combination of these aspects to form a complete relaying system for the protection of transmission lines will now be given. Before going into the specific details of the three example systems, there are some fundamental characteristics which should be discussed.

It is the main concern of a protective relaying system to detect and remove faults as quickly as possible to prevent equipment damage. Also a secondary requirement is to accomplish the fault removal with as little disruption to the power system as necessary. To accomplish these objectives any protective system must answer the following three questions:-

1- Is there a fault?
2- Where is the fault?
3- Should a trip signal be issued?

The three questions are usually combined through the relay scheme which reduces them to the one question:-

1- Is there a fault within the zone of protection?

If the answer is yes, then a trip signal is issued to the appropriate circuit breaker, otherwise nothing is done. The single question is equivalent to the three, but as will be shown later, it is often useful to consider the three separately.

The transmission line relaying system can be characterized as a circuit breaker opening control system used for protection. It is always located at the ends of the transmission line at the substation where the circuit breakers are located. The decision for this control system must be made based on the information available at each substation. This information resides primarily in the current and voltage signals from the transmission line end at the substation although there is often (especially at higher voltages) a communication signal from the other end of the transmission line.

The requirements for a digital relay protecting a transmission line can be broken into three parts. The first is to obtain the necessary information from the currents and voltages at the local substation along with the communication signals from the remote substation. Then the digital relay must process that information to determine the existence and location of any faults. Finally, the digital system must decide whether or not to issue the appropriate signals to open the local circuit breakers and also to send the appropriate signals via the communication link to the remote substation at the other end of the line. From a system point of view the three requirements can be characterized as data acquisition, fault algorithm, and relay logic scheme. Now to examine the three digital relays.

PRODAC 70 PROJECT

This project, a joint Pacific Gas & Electric - Westinghouse effort, evaluated the performance of an experimental hardware/software computer system functioning as one terminal of transmission line protection. The performance was evaluated in the laboratory with a 600 v miniature power system as well as in a field installation which included staged fault tests.

For an overall view of the system, consider the diagram in Figure 1. The ac data from the power system passes through the signal conditioning unit (which isolates, filters, and scales the data) to the analog to digital (A/D) subsystem where it is sampled and converted. With the completion of the conversion, the data moves from the scratch pad memory (SPM) into the computer memory under program control. A typewriter and programmer's console provide facilities for logging of desired data as well as a means for executive control, software generation, program loading, modification, and checkout. The contact outputs were used for reclosing (in the laboratory) and the operation of various alarms. A high speed output for circuit breaker tripping is also provided.

The computational unit for the project was a Westinghouse P-2000 process control computer which included standard software such as an executive, an input-output control section, interrupt handler, as well as programmer support and library. The key PRODAC 70 software development was the relaying program which is shown in Figure 2.

A service request interrupt (SRI #5) is initiated by an A/D completion signal after each sample. This program runs with the highest priority. A series of 9 channel inputs reads the sample set and stores it in raw data tables. An out-of-step check is made, then the data tables are updated. With these tables, data surrounding a fault, both before and after, can be reserved for later logging.

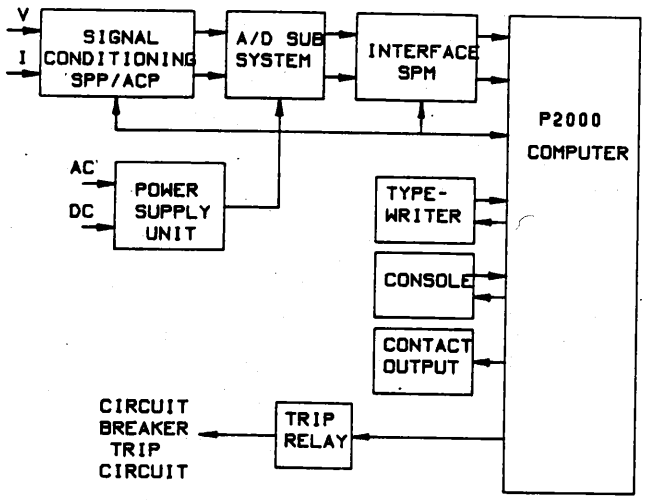


FIGURE 1 PRODAR 70 SYSTEM BLOCK DIAGRAM

During non-fault conditions, the fault program is inactive and a disturbance check is made to determine if a fault has occurred. This is the first of the three questions mentioned before. Ground fault detection is made by checking the residual current. The phase fault detector makes predictions of the values of each phase current based on previous values. Since the sampling is asynchronous, prediction must be made by a mathematical combination of values and their rates of change. If deviation between prediction and present values is observed, the phase fault detector operates to start the fault program. If no indication of a disturbance is found, the interrupt program returns control to the lower priority program which was interrupted by the SRI #5.

If either the ground or phase fault detector programs operate, the fault program shown in Figure 3 is executed. With the requirement to locate the fault based on phasor impedance calculations which are time-consuming, a fault type analysis program (FTA) determines which phase or phases are involved in the fault. A pair of high phase currents, or high current on a single phase and residual, or collapsed potential on a particular phase or phase pair, provides such an indication. Also very high magnitude currents can initiate instantaneous high-set overcurrent tripping at this point. If the FTA finds clear symptoms of which phase or phases are faulted, it proceeds directly to zone-2 and zone-1 phasor impedance calculations. If no clear indication exists, the fault program makes a long range zone-3 impedance check on all pairs to see if any are faulted. If the zone-3 check locates a faulted pair, it is processed by the zone-2/zone-1 logic. Location of a fault within zone-2 is recorded for later logging; a zone-1 location initiates tripping of the circuit breaker. After any of these actions, or even if no fault is found, a broad impedance-based clearing check is executed. A fault within the clearing check zone results in a return to the zone-3 check; otherwise the fault program is terminated. Repeated loops between the clearing check and distance measuring programs will result in a breaker failure logging where tripping was attempted; otherwise failure of external relays is noted.

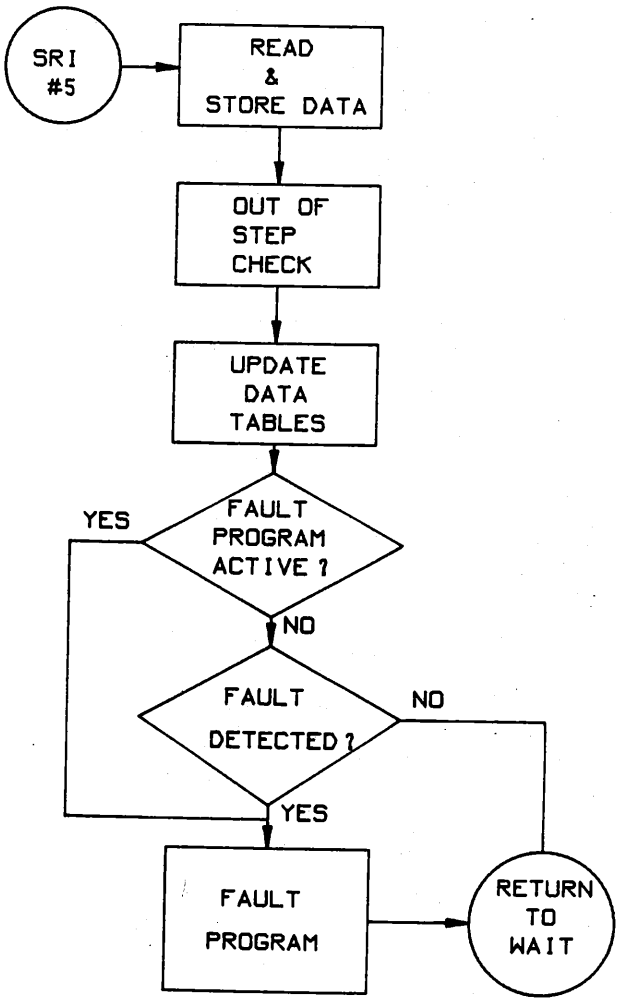


FIGURE 2 PRODAR 70 OVERALL RELAYING PROGRAM

The distance programs compare the calculated phasor impedance to zone limits described by the R-X reach characteristics of Figure 4. The impedance value in effect answers the question about the location of the fault. Comparison with the R-X characteristic decides whether a trip signal should be issued. The particular characteristic shown was tailored for the field installation. The extended zone-2 and

zone-1 reach in the R direction accommodates high ground fault resistance encountered in the particular field installation. The zone limits are stored as angle-indexed tables of impedance limits. This follows from the polar form of the impedance algorithm output. With different tables virtually any appropriate shape can be generated.

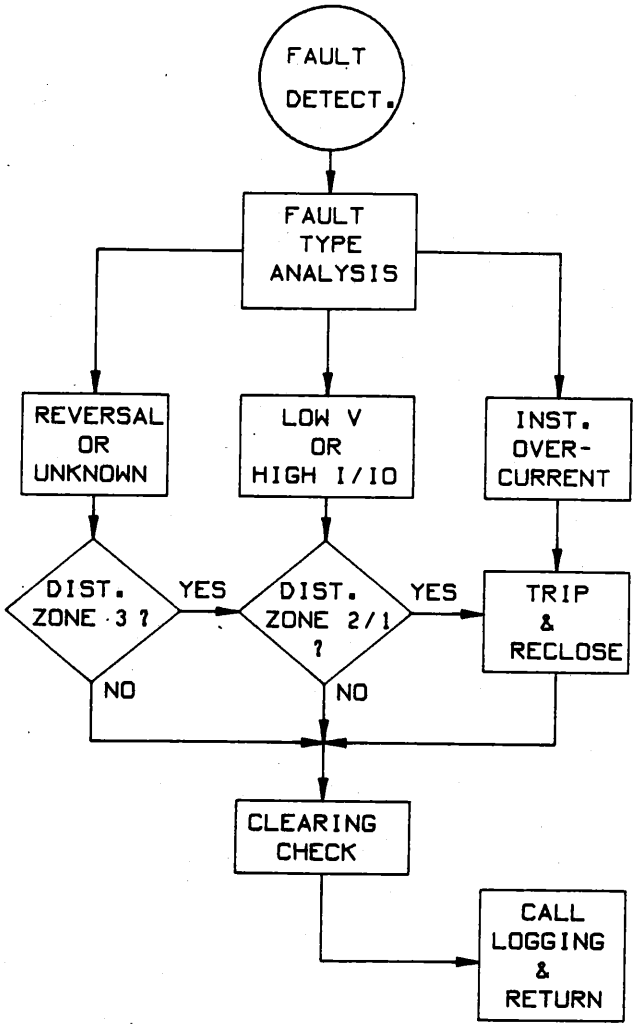


FIGURE 3 PRODAR 70 FAULT PROGRAM

To illustrate how the various parts of the system are integrated into a compatible and optimum whole, the algorithm for the impedance calculation is now reviewed and its effect examined. The apparent impedance is found with the following equations

$$Z^2 = \frac{V_{pk}^2}{I_{pk}^2} = \frac{v'^2 + v''^2}{i'^2 + i''^2}$$

$$\theta = \tan^{-1}\left(\frac{i'}{i''}\right) - \tan^{-1}\left(\frac{v'}{v''}\right)$$

where

v'=1st divided difference of voltage
v"=2nd divided difference of voltage
i'=1st divided difference of current
i"=2nd divided difference of current

The divided differences of the voltages and currents are found from the sampled data by:

$$v_k' = \frac{1}{2h\omega}\left(v_{k+1} - v_{k-1}\right)$$

$$v_k'' = \frac{1}{h^2\omega^2}\left(v_{k+1} - 2v_k + v_{k-1}\right)$$

where h is the sampling interval, and the k-1, k, k+1 subscripts refer to a set of consecutive samples. Now here is an example of the interaction of the algorithm with the rest of the system. In the above equations, division by $h\omega$ is indicated, which could be time-consuming. However, if the ratio, $1/h\omega$ were made equal to 2, the division operation merely becomes a shift operation on the binary computer. This is what was done, and the sampling time is set to 1.326 ms in order to simplify the calculation.

The above formulas use first and second divided differences in order to minimize errors from subnormal frequencies associated with slowly decaying transient dc offsets as well as from the series capacitors adjacent to the protected line. Higher frequency transients are now accentuated, so hardware (filter) and software (integration and repetition) techniques are needed to reduce the deleterious effects of the extra differentiation.

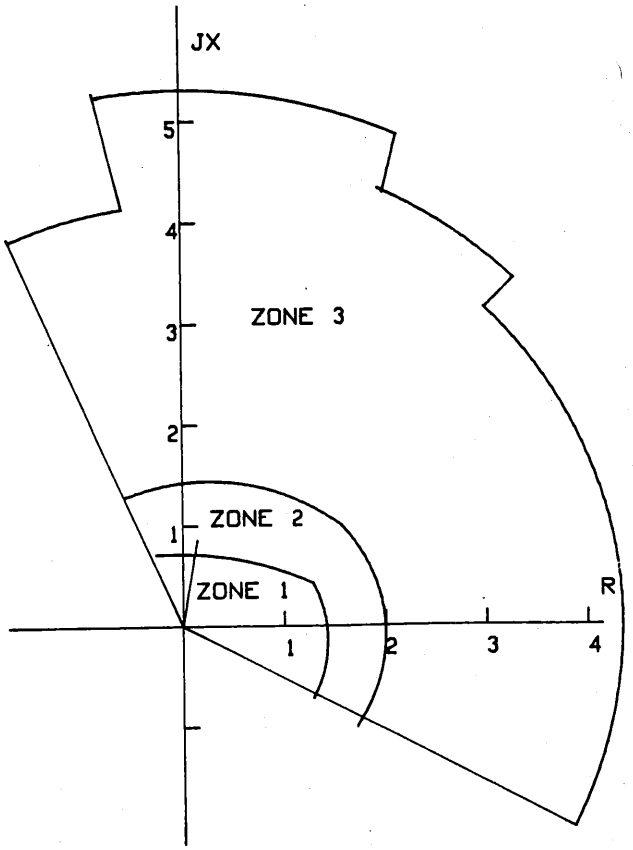


FIGURE 4 PRODAR 70 R-X CHARACTERISTIC

The preceding hardware and software descriptions have briefly summarized the system design. References [24] and [25] give a complete description of the hardware, software, and application considerations. They also describe comprehensive model power system tests which assessed the accuracy, surge-withstand capability, and the relaying performance of PRODAR 70.

```
 9/ 9/73 PRODAR 70 LOGGING EVENTS AT
   2 HR. 12 MIN.  6 SEC.
GROUND FAULT DETECTOR OPERATED; SKCNTR = 4794
FTA FOUND HIGH CURRENT ON RESIDUAL & PHASE C,
TIME =  12 MSEC.; SKCNTR =  4802
ZONE 2 GROUND DISTANCE OPERATION, PHASE C,
LAST APPARENT IMPEDANCE - 1.7 OHMS AT 78 DEGR
TIME =  18 MSEC.; SKCNTR =  4806
ZONE 1 GROUND DISTANCE TRIP, PHASE C,
FAULT APPROX. 18.2 MILES FROM THIS POINT
LAST APPARENT IMPEDANCE - 1.7 OHMS AT 78 DEGR
TIME =  23 MSEC.; SKCNTR =  4813
EXTERNAL RELAY OPERATED,
TIME =  41 MSEC.; SKCNTR =  4831
ZONE 2 GROUND DISTANCE OPERATION, PHASE C,
LAST APPARENT IMPEDANCE - 1.7 OHMS AT 78 DEGR
TIME =  99 MSEC.; SKCNTR =  4889
ZONE 1 GROUND DISTANCE TRIP, PHASE C,
FAULT APPROX. 18.2 MILES FROM THIS POINT
LAST APPARENT IMPEDANCE - 1.7 OHMS AT 78 DEGR
TIME =  99 MSEC.; SKCNTR =  4889
EXIT FROM RELAYING LOGIC,
TIME = 122 MSEC.; SKCNTR =  4912
PHASE FAULT DETECTOR OPERATED; SKCNTR =-15864
FTA FOUND NO SEVERE CONDITIONS,
TIME =  18 MSEC.; SKCNTR =-15850
EXIT FROM RELAYING LOGIC,
TIME = 171 MSEC.; SKCNTR =-15697

RECORD    11 MEDIANS OF PEAKS:
RESERVED TABLE 1 @ 233D
IA -   0.64 AMPS.
VA -  93.33 VOLTS
IB -   0.62 AMPS.
VB -  93.78 VOLTS
IC -   0.59 AMPS.
VC -  93.37 VOLTS
IR -   0.09 AMPS.
RESERVED TABLE 2 @ 23C2
IA -   1.44 AMPS.
VA -  94.39 VOLTS
IB -   1.76 AMPS.
VB -  94.07 VOLTS
IC -  31.47 AMPS.
VC -  92.67 VOLTS
IR -  28.11 AMPS.
```

FIGURE 5 PRODAR 70 LOGGING OF 9/9/73 FAULT

The PRODAR 70 system was installed on a 230 kv line at PG&E's Tesla Substation in 1971 and has been in operation since then. PRODAR 70 has correctly ignored all external faults and has never given an indication of false tripping for any reason. The system also experienced a number of internal faults, both natural and staged. Here also the performance was excellent.

As an example, the response to a natural fault which occurred on September 9, 1973 is reviewed. The logging of this fault is shown partially in Figure 5. Oscillograms of the fault were also recorded to indicate the ac data processed by the system as well as monitoring the computer trip output which shows tripping in about one and a half cycles. The computer was not connected to actually trip the breaker; line protection was provided by conventional relays.

The log shows the steps taken by the relaying software. The ground fault detector operated in response to residual current and initiated the fault program. The ground fault detector program requires about 4 ms to operate and the FTA took another 8 ms to determine high current only on phase C with high residual current which indicates a C-G fault. This is logged at 12 ms.

The ground distance program then calculated the impedance and compared the results to the stored zone limits. The distance program classified the fault as zone 2 and logged it at 18 ms. At 23 ms, the program located the fault within zone 1 and issued a trip signal. Using the calculated impedances, the program also determines an approximate distance in miles to the fault. The next entry shows operation of the conventional pilot relay system, designated here as the external relay. The 41 ms time consists of 39 ms trip time and 2 ms for response of interfacing hardware.

With the delay in the tripping of the conventional relays and the delay in breaker clearing, the software clearing check does not immediately see clearing and forces a return to the distance program. The zone 2 - zone 1 ground distance programs repeat their previous interpretation and issue another trip signal at 99 ms. Finally at 122 ms, the relaying program is satisfied that the fault is gone and exits. However, reclosing causes the phase fault detector to operate and the relaying program makes another pass. The fault has been successfully cleared and there are no indications from the distance program until the relay program exits at 171 ms. Also shown is the analysis of one of the reserved fault data tables.

In 1974 the PRODAR 70 system was subjected to a series of eight staged faults on the protected line. The computer performed primary protection and was actually connected to trip the breaker. The performance of the system was gratifying; it tripped in 20-23 ms for every fault. The tests also provided new data on the specific responses of the relaying programs to dc offsets, c.t. saturation, and mutual effects due to parallel lines.

In summary, the operation of this digital relay system has been excellent. The hardware used in the PRODAR 70 system was selected for convenience and suitability for experimental development work rather than as a commercial prototype. Nevertheless, hardware performance in the field has been more than satisfactory. Field experience with the PRODAR 70 system has firmly established the technical feasibility of computer relaying.

GENERAL ELECTRIC - PHILA. ELECTRIC PROJECT

The General Electric Co. and the Philadelphia Electric Co., established a joint project in 1973 to investigate the feasibility of using digital techniques for the protection of transmission lines. The basic plan was to use two minicomputers, one at each end of a 500 kV transmission line, to explore the operation of a digital relaying system. Explicit points of interest were the operating speed, the dependability, and the security of the relaying system. The goal of the project was to develop relaying algorithms and implement them with available digital hardware. The objective of the digital protection system was to equal or surpass the performance of existing relay systems and to provide added functions possible through digital techniques.

The project was divided into three phases. The first involved a single minicomputer terminal in an extensive laboratory investigation. The second phase was another laboratory investigation involving two terminals with a communication link which explored a directional comparison relaying scheme. The third phase was the field installation of the two terminals at the ends of a 116 km (72 mi), 500 kV transmission line on the Philadelphia Electric Co. system. The field installation was in operation for one year in a monitoring mode with no actual tripping of the circuit breakers. During that year, staged fault tests were made to demonstrate the operation of the system. The field test was terminated in June 1978.

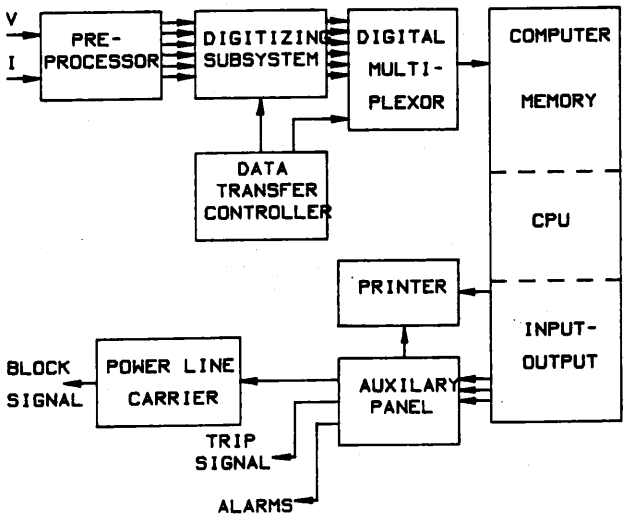


FIGURE 6 GE/PE SYSTEM BLOCK DIAGRAM

Hardware Considerations

A single terminal of the system, as shown in Figure 6, consists of several distinct functional blocks. Six continuous signals, the three phase currents and the three phase voltages, are supplied by the transmission system to the preprocessor. A chain of amplifiers in the preprocessor scales the voltage signals to a range suitable for the digitizing subsystem. Current transformers, on the line side of the circuit breaker, provide the secondary line currents. The current signals pass through isolation transformers and auxiliary current transformers with shunts to convert them to proportional voltage signals. These are fed into the preprocessor of the digital system.

The data transfer controller sets the sampling rate of the digitizing subsystem. A sampling rate of 16 samples per cycle (960 samples per second) was chosen after considering the time required for calculation between samples. Six analog signals are sampled simultaneously, held and converted into digital numbers by six independent channels of analog to digital converters. The converted signals are stored in 14 bit buffer registers until, upon completion of the digitizing process, they are transferred directly into computer memory. The total time for the conversion and transfer is approximately 110 microseconds. After one set of six power system signals is transferred, a high priority interrupt is initiated to start the data handling and fault executive programs.

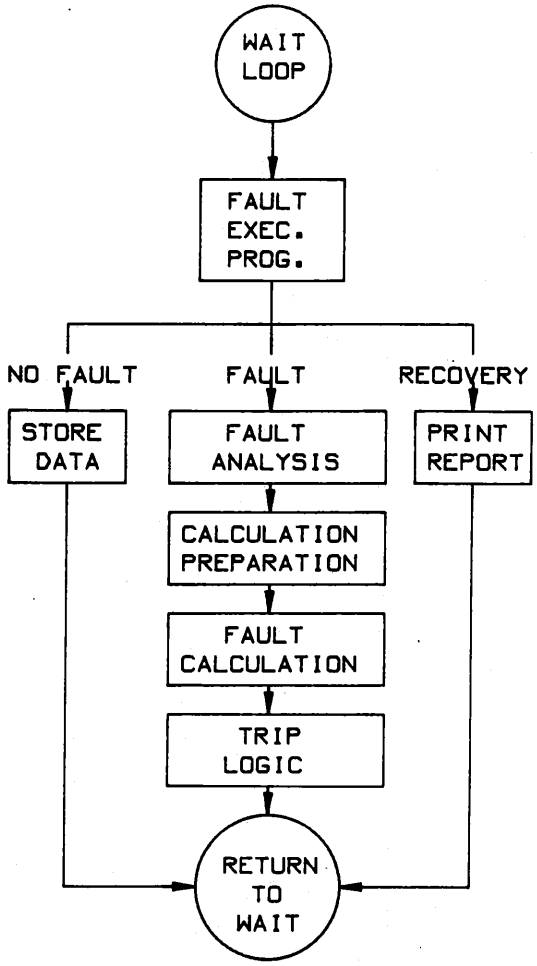


FIGURE 7 GE/PE FAULT PROCESSING FLOW CHART

Software Considerations

The program organization incorporating the software requirements of the system is shown in Figure 7. The computer program is normally executing the wait loop until the data input interrupt indicates that a new sample of data has been entered into memory by the data acquisition system. It is the task of the fault executive to determine which of the states, no fault, fault, or recovery is to be executed. The program detects a fault by comparing the latest set of sampled data with the corresponding set in memory obtained one cycle previously. Since the sample rate is 16 times a cycle, there is no need to make predictive calculations as in PRODAR 70 since values will correspond from cycle to cycle. This is the primary reason for selecting a fixed number of samples per cycle. If the two sets differ, the executive calls on the fault processing system which determines the fault type, selects the appropriate combination of voltages and currents, performs the basic fault calculation algorithm, and finally decides whether to trip or not. Following a fault, the fault executive monitors breaker current or time to decide if the system is recovering and after printing a report returns to the original no fault state.

The fundamental algorithm determines the fault location by finding the circuit parameters, R and L, from the system differential equation,

$$v = Ri + Ldi/dt$$

The values of v, i, and di/dt can be approximated from the incoming data and the values of R and L are then calculated with the above equation.

One of the major constraints on the program is the limited time to make a trip decision. Since the basic algorithm calculation consumes a major portion of the available time between each sample, the program must select the correct fault type and restrict its calculation to that particular fault. A separate algorithm for fault analysis using the phase currents and Clarke components was developed for this purpose.

Directional Comparison Trip Logic

The original laboratory investigation used a single computer at one end of the line. With such an arrangement, a two zone stepped distance relay scheme was used for the trip logic. However later phases of the project used two terminals and a directional comparison blocking scheme was used. This latter scheme will be discussed.

The trip logic routine first determines if the calculated values of R and L lie within the tripping or blocking zones of the relaying characteristic. Actually as seen in Figure 8 there are different relaying characteristics for various fault types. The sloping down of the 1st zone characteristic for phase to ground faults was necessary to take care of the effects of load and fault resistance. By the use of sample counts various time delays are introduced in order to implement the logic. For high speed tripping, the trip signal is issued after four calculations are located within the first zone. This corresponds to a minimum trip time of 6.1 to 7.4 milliseconds. All external faults determined to be within the blocking zone for two consecutive fault calculations will start carrier transmission to block the remote terminal from tripping. Four consecutive R and L calculations within the overreaching pilot zone indicate a fault that may or may not be on the protected line. An additional count of six samples is used to permit coordination with the communication channel and the blocking time at the remote terminal. After this delay, the trip signal will be issued unless blocked by a signal received from the remote terminal.

A ground fault directional supervisor is also included in the fault processing for single phase to ground faults. This routine was added to detect faults with high resistance that are outside the conventional zone characteristics. Also under some system conditions, fault resistance can cause external phase to ground faults to appear in the second quadrant of the R,L diagram or the first zone characteristic. For this reason, the ground fault directional supervisor is also used to block first zone tripping when reverse faults are detected.

There is a close-in directional calculation using pre-fault voltages which is used for faults which are found to be close to the relaying terminal by the "L" calculation. This routine prevents incorrect tripping caused by calculation error from low voltage data and overcomes problems caused by the transient response of CVT's during close-in faults.

TABLE I

TYPICAL TRIP DATA
NUMBER OF SAMPLES TO TRIP*

FAULT TYPE		FAULT LOCATION (MILES) 0	8	40
3 Phase	Avg.	6.78	6.71	6.80
	Min.	6	6	6
	Max.	13	9	10
B-C	Avg.	6.31	6.38	6.13
	Min.	6	6	6
	Max.	7	9	7
A-G	Avg.	6.19	6.31	6.31
	Min.	6	6	6
	Max.	9	8	9
B-C-G	Avg.	9.00	9.00	8.11
	Min.	6	6	6
	Max.	15	16	13

* 1 Sample = 1.04 milliseconds

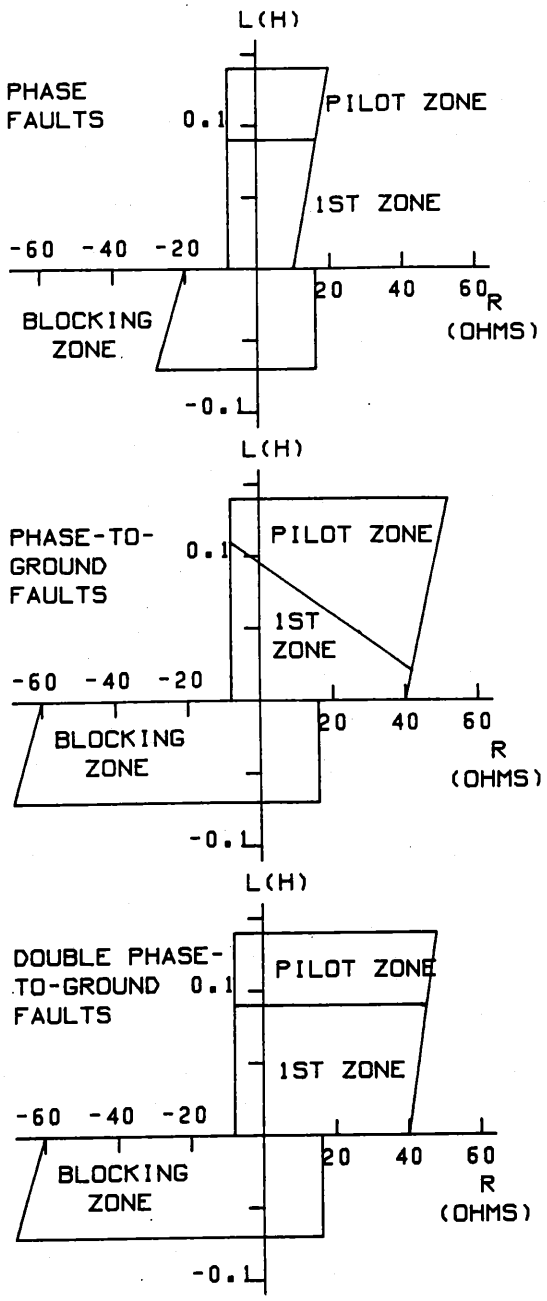


FIGURE 8 GE/PE ZONE CHARACTERISTICS FOR DIFFERENT FAULT TYPES

Test Results

Some of the various test results are shown in Tables I, II, III, and IV. These tables summarize some of the results from the one and two terminal laboratory investigations as well as the field tests.

In the original single terminal investigation, it was important to determine the basic characteristics of the fault algorithm as well as the whole concept of digital protection of a transmission line. Consequently 8000 laboratory tests were made covering all types of faults applied at numerous locations both internal and external to the protection zones. Fault incidence angles were varied over a range of 0 to 180 degrees and various power transfer angles were also used. The performance of the system is best summarized by a review of the trip times as shown in Table I.

The consistency of the trip times observed throughout the protected zone was encouraging. By examining the average values of the trip time, it can be seen that tripping is usually initiated in six or seven samples. This reduces to trip times of from 6.12 to 8.44 milliseconds so that tripping is usually less than a half cycle. From the maximum values, the worst case trip times are one cycle or less.

TABLE II

TYPICAL BLOCK/TRIP TIMES
TWO TERMINAL TESTS

FAULT TYPE		BLOCK TIME (ms) BLOCKING ZONE	TRIP TIME (ms) FIRST ZONE (CLOSE-IN)	TRIP TIME (ms) PILOT ZONE END OF LINE
3 Ph	Avg.	6.02	8.46	15.1
	Min.	5	7	13
	Max.	8	14	19
B-C	Avg.	6.02	7.65	15.21
	Min.	5	7	13
	Max.	7	9	18
A-G	Avg.	5.31	7.45	15.34
	Min.	4	7	13
	Max.	8	10	21
B-C-G	Avg.	7.91	11.38	18.16
	Min.	5	7	13
	Max.	15	16	28

Table II shows some results from the two terminal laboratory investigation. In testing this directional comparison scheme, the faults of primary interest were internal faults at the line ends and external faults within the pilot zone reach of the remote terminal. From Table II it can be seen that, except for double phase to ground faults, the average trip time for close in faults is less than a half cycle. The maximum trip time for all close in faults was less than one cycle. For line end faults, the average trip time was less than one cycle for all but the double phase to ground faults, even with the delay introduced for communication channel coordination. The blocking signal was usually initiated in 6 milliseconds or less for external faults in the reverse direction.

During the field investigation there were correct operations for all 15 external faults detected by the digital system. The blocking signal times are shown in Table III. All external faults were phase to ground and only three faults, #2, #3, and #13 were on the 500 kv system. The remainder were faults on the 230 kv system.

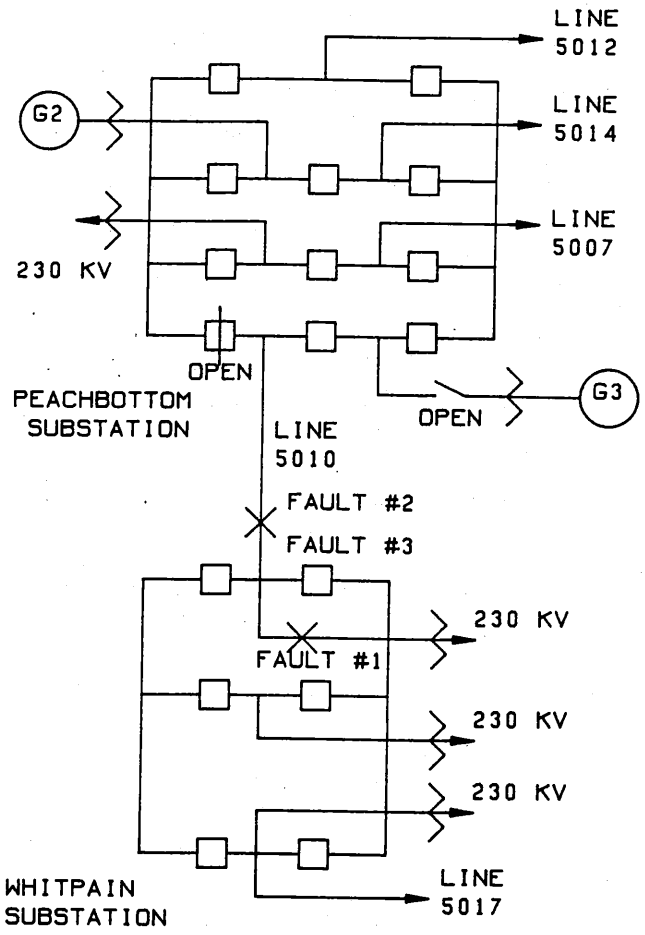


FIGURE 9 GE/PE 500 KV SYSTEM DURING STAGED FAULT TESTS

During the field investigation staged fault tests were made on the 500 kv line for the primary purpose of checking the digital protection system. Three internal faults were staged. Figure 9 shows the transmission system setup and the location of the faults. For the first test, a B phase to ground fault was applied at the Whitpain terminal. The 2nd and 3rd tests were an A phase to ground fault and a B phase to C phase fault. These were applied at a tower 72.6 km (45.1 miles) from the Peach Bottom terminal. Table IV shows the tripping speed of the digital system. It should be noted that the digital system did not perform the actual tripping; the existing primary and backup relays tripped the line circuit breakers. Without exception, the digital system operated faster than the existing primary and backup relays. The digital system at Whitpain terminal operated near minimum time, less than a half cycle. The digital system at Peach Bottom was somewhat slower.

One of the interests in digital relaying is its ability to supply some added functions. In this project, one of these functions was the report giving the results of the operation. Figure 10 shows the Peach Bottom report for the 2nd staged fault test. Besides the usual logging of date and time, there is an estimate of the distance to the fault, the type of fault, the relay operation time, the breaker clearing time, and the RMS value of fault current. This information represents some of the added benefits which a computer can supply.

TABLE III

OPERATIONS DURING EXTERNAL FAULTS*

FAULT NUMBER	RELAYING LOCATION	BLOCKING TIME (ms)	FAULT LOCATION#	STATUS OF REMOTE TERMINAL
1	W	7	2	A
2	PB	5	0	B
3	PB	6	1	B
4	W	6	3	C
5	PB	18	?	A
6	W	5	3	C
7	W	5	2	A
8	W	8	3	C
9	W	11	1	B
10	W	12	1	D
11	W	5	1	D
12	PB	6	2	C
13	W	12	1	C
14	W	5	1	A
15	W	5	2	A

*All faults were single phase to ground
Number of buses between relay and fault

W - Whitpain
PB - Peach Bottom
A - Fault not detected
B - Digital system off line
C - Detected fault - current below trip level
D - Blocked by carrier signal

```
FAULT OCCURRED APR  6 1978    11:49:32
FAULT AG
DISTANCE TO FAULT   44.8 MILES
TRIP TIME    .44 CYCLES  ( 7.29 MSEC)
FAULT CURRENT   5223 AMPS (RMS)
CLEARING TIME   3.56 CYCLES
 SAMPLE        R          L          TYPE
   1           *          *          AG
   2           *          *          AG
   3           .8         .0853      AG
   4           5.1        .0600      AG
   5           5.1        .0738      AG
   6           4.9        .0719      AG
   7           5.1        .0724      AG
   8           3.5        .0695      AG
   9          12.2        .0729      AG
  10           2.6        .0785      AG
  11           3.8        .0755      AG
  12           5.5        .0678      AG
  13           5.5        .0691      AG
  14           6.7        .0752      AG
  15           3.5        .0676      AG
  16           7.0        .0700      AG
```

FIGURE 10 GE/PE REPORT AT PEACH BOTTOM SUBSTATION - 2ND FAULT

Conclusions of the GE/PE Project

The objective of the digital protection system project was to develop techniques and algorithms for a relaying system that equalled or exceeded the performance of existing solid state relaying systems and also offer some added functions. The digital protection system project met its objectives and successfully demonstrated the capability and performance of digital techniques for transmission line protection. Papers on this project are included in References [66], [85], and [90].

TABLE IV

TRIP TIMES - STAGED FAULT TESTS
(milliseconds)

	DIGITAL SYSTEM	PRIMARY RELAY (SOLID-STATE)	BACKUP RELAY (ELECT-MECH)
TEST #1 (B-G AT WHITPAIN)			
PEACH BOTTOM	23	30	-
WHITPAIN	8	21	27
TEST #2 (A-G AT TOWER)			
PEACH BOTTOM	10	26	47
WHITPAIN	7	20	26
TEST #3 (B-C AT TOWER)			
PEACH BOTTOM	14	34	22
WHITPAIN	7	33	20

AEP DIGITAL RELAY PROJECT

This project began in 1971 with a joint research project with IBM Corp. This phase of the project which lasted about one year was a feasibility study of a substation computer system. The major portion of that effort concentrated on developing programs for distance relaying of transmission lines.

This original phase of a continuing research effort used an IBM System 7 minicomputer. This system was installed in the field. Programs developed in the laboratory and tested were:

1. Alarm monitoring and data logging
2. Control
3. Oscillography
4. Relaying

The field installation in Virginia included a teleprocessing link to another computer in AEP's New York office.

The relaying function included many different specific functions for transmission line protection such as:

1. Three zone distance relaying and high set current relaying for phase faults.
2. Directional overcurrent, instantaneous, and inverse time protection for ground faults.
3. Breaker failure protection
4. High speed and automatic reclosing logic with appropriate synchronization checks.
5. Carrier logic.

Much of the original algorithms and software was based upon the work of Mann and Morrison, and the PRODAR 70 project. This part of the project is reported in Reference [62]. But after a substantial amount of investigation, it was decided to abandon the type of algorithm which is based on polynomial type approximations and concentrate on a digital harmonic filter. With this decision, many different approaches and procedures were developed.

Again in this project, there are many examples of the possible tradeoffs between the hardware and software and how the different facets of the digital system interact with each other. With the adoption of the digital harmonic filter, it was found that the decaying dc offset must be removed prior to executing the filter calculations. The use of mimic circuits to accomplish this is well known in relaying literature. Such circuits represent additional characteristics for the required analog filters. The digital filter equations were designed to operate on 12 samples per cycle. This is a very convenient sample rate since the filter coefficients reduce to positive and negative values of 0, 1/2, 1, and $\sqrt{3}/2$, so that only one irrational coefficient is needed. There are, of course, numerical methods to represent irrational numbers, for instance, a binary series of four terms. But the procedure chosen was to again change the analog input, and bring into memory the variable modified by the appropriate coefficient. This additional complication in the input system was offset by the improved advantage to the calculation requirements. Probably more important than the changes mentioned above, this different approach opened up the possibility for a significant new attack on the technique for distance relaying.

Distance Relaying with Symmetrical Components

Symmetrical components are one of the basic tools of analysis available to a power engineer. Nowhere has the impact of symmetrical component theory been greater than in the area of power system fault analysis and in the related fields of relaying and protection.

It is well known that on a grounded three phase power system ten different types of fault may occur: 3 phase to phase, 3 phase to ground, 3 double phase to ground, and 1 three phase fault. Present three phase distance relaying systems normally employ six impedance measuring units. The units act in parallel and under any fault condition the appropriate unit will act to provide the necessary tripping logic. In the digital relay version, a similar approach would require that the impedance measuring algorithm must be executed six times for each sample. It has been the approach to utilize a

fault analysis algorithm to determine the type of fault and then use the impedance algorithm for that one fault. This was the technique of the PRODAC 70 and GE/PE projects.

The most significant feature of the AEP symmetrical component approach is that a single performance equation for all faults has been developed. This effectively eliminates the need for fault type identification for the distance relaying function. The required values for this single equation consist of the symmetrical components of line to neutral voltages and line currents. With the use of a fundamental frequency digital harmonic filter, the various components are determined by an appropriate selection of the filter coefficients. Thus the use of the digital filter prompted and permitted the final development of this approach.

The operating equation of the system is given by:

$$k = \frac{k_1 + k_2 k_2' + k_0 k_0'}{1 + k_0' + k_2' + k_L} + \varepsilon_R$$

where k_0, k_1, and k_2 represent ratios of zero, positive, and negative components of voltages with appropriate IZ drops. The terms k_0', k_1', and k_2' are other ratios or parameters that help to reduce the various fault conditions to the single equation.

The symmetrical component calculation involves a Symmetrical Component Discrete Fourier Transform process (SCDFT) which utilizes the 12 sample per cycle data. The procedure for voltages is shown below (a similar procedure is used for the currents).

$$E_0 = \frac{1}{3} \sum_{k=0}^{11} w_k (e_{Ak} + e_{Bk} + e_{Ck})$$

$$E_1 = \frac{1}{3} \sum_{k=0}^{11} w_k e_{Ak} + w_{k-4} e_{Bk} + w_{k+4} e_{Ck}$$

$$E_2 = \frac{1}{3} \sum_{k=0}^{11} w_k e_{Ak} + w_{k+4} e_{Bk} + w_{k-4} e_{Ck}$$

$$w_k = \frac{j}{6\sqrt{2}} \epsilon^{-\frac{jk\pi}{6}}$$

k = kth sample of e(t)
e(t) = instantaneous value of voltage

With the above components, the appropriate ratios are calculated and substituted into the operating equation. The error term, ε_R, which includes the effects of fault resistance, is assumed to be negligible. The computed value of k is then positioned on the relay characteristic to obtain the relay response to the prevailing condition. Additional information can be found in Reference [69].

Present and Future Work

The above procedure has been checked out in the laboratory and is now being implemented into a complete substation computer system for field installation.

Although this discussion is primarily about transmission line relaying, it may be well to point out how a digital relay may fit into a complete system. The four blocks that will comprise the total protection and control system are:

1. Line relaying and associated control
2. Transformer relaying and control
3. Alarms and data logging
4. Host computer

The arrangement is shown in Figure 11 and the various blocks will utilize available micro-computers.

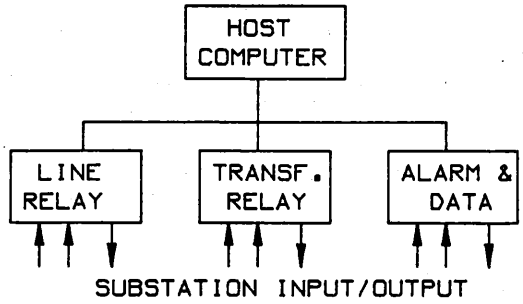


FIGURE 11 AEP SUBSTATION COMPUTER SYSTEM

The basic structure for a standalone relay system is shown in Figure 12. The building blocks for line relaying are-

1. Computer interface:
   Consists, mainly, of analog circuitry for surge protection, filtering, and scaling for both voltage and currents. It will contain the mimic circuits to remove the dc offset from the fault currents.

2. A/D subsystem:
   This will contain the converters to create the digital information from the analog signals. Also a means for entering data directly into computer memory will be provided.

3. SCDFT:
   The symmetrical component calculation.

4. Fault processor:
   The single operating equation will be evaluated. The relaying logic, circuit breaker failure logic, and the reclosing logic will be included.

The other components of the substation computer system will be similar with differences dictated by the functions assigned to them. As an example, the SCDFT will not be needed for the alarms and data logging processor, but more input/output will be required.

Although the AEP project is a continuing effort, several conclusions have been drawn from the previous work. It is definitely a technically feasible concept to use small computers to perform substation tasks including the protection function. The main

effort remaining is to continue with a demonstration of a substation computer system under the severe substation environmental conditions.

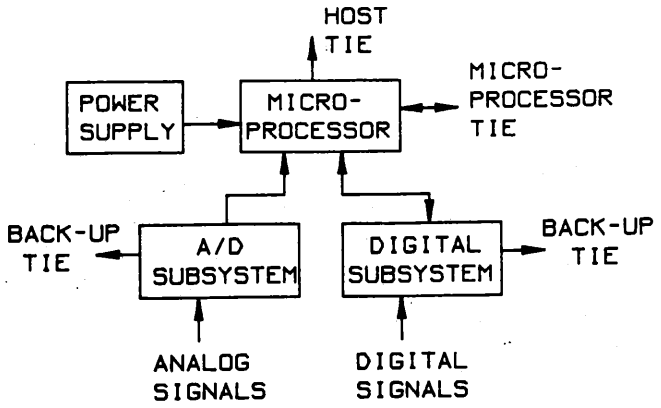


FIGURE 12 AEP RELAY COMPUTER

SUMMARY

This presentation has covered three different projects for the protection of transmission lines by digital methods. Although there are essential differences, for instance, there are three completely different algorithms, there are many similarities. All systems bring instantaneous values of current and voltage into memory via analog to digital converters. The computers in each system then perform calculations on the incoming data in order to obtain distance estimates to the fault. These distance estimates are either a polar form of impedance, the values of the circuit parameters, R and L, or a value, k, actually representing the ratio to total line length. These distance estimates are then used on a relay characteristic to make the final decision of whether to trip a circuit breaker or not.

It can be said that, based on these presentations, there are new techniques, the digital computers, for example, but they are still used within the traditional protection philosophy, which, for transmission lines, is distance protection. These projects are good examples of how technological progress should be made. New ideas and techniques should be incorporated and used with the time-tested philosophies which have demonstrated success. New philosophies will evolve, no doubt, but in this initial phase of development, it is desirable to build on the successes of the past.

CHAPTER V

LINE PROTECTION II - UNCONVENTIONAL APPROACHES

Many times, the motivation to consider an unconventional approach stems from the need for additional functions such as fault location, increased selectivity, increased sensitivity, high speed and self-checking. High speed fault detection can require a non-conventional approach to meet desired objectives.

The types of faults such a system should be capable of detecting are as follows:

1. Momentary, or transient, faults: an example of this type of fault is a lgihtning flash over an insulator. This leaves no permanent damage, and successful reclosure of circuit-breakers is possible. However, these faults should be located to facilitate inspection, and also for purposes of data collection for future designs.

2. Sustained, or permanent faults: these include grounded conductors, as well as open and short circuits at all levels of test voltage. Successful reclosure of circuit breakers is not possible, and the system is "down". This type of fault must be repaired as soon as possible to put the system back into operation.

3. High-breakdown faults: these appear as faults only at high voltages. An example would be a fallen line that is close to, but not actually touching, the ground. This creates an arcing ground and makes successful reclosure of circuit breakers impossible. High-breakdown faults can be considered permanent as they must be cleared before system operation can be restored.

4. Latent faults: these are localized impairments which do not prevent successful operation under normal conditions. However, the design insulation margin for surges and dynamic overvoltages is degraded. This is a condition that deteriorates with time and should be located with preventive maintenance in mind.

Unconventional techniques of detecting fauls fall into two general categories: 1) active approaches and 2) transient approaches. A list of the possible techniques under each of these categories is given below.

I. Active Approaches

- Pulse Radar
- Frequency Modulated Sweep

II. Transient Approaches

- Discontinuity Detector
- Traveling Wave Discriminant
- Frequency Transient

Many of the techniques listed above are ideas that have been proposed by various researchers and are not yet tested and verified. Some of the above techniques have been studied in some detail but have not been fully tested in a laboratory or subjected to field tests. If a utility decides to embark on an implementation of an unconventional technique then the particular technique chosen must be thoroughly tested and studied.

Primarily, the above schemes involve digital computation devices. The rapid development of microprocessors makes it possible to implement protection schemes economically that were not possible in the past. The increased computational capability does allow new and sophisticated techniques to be developed. New techniques should now be studied and developed rather than only considering digital implementation of conventional protection techniques. The potential exists for increased function, greater accuracy, higher speed, low cost, high reliability and self checking.

The Substation Computer Working Group of the IEEE Relaying Committee recently compiled a list of functions that could be performed by a substation computer. This list is shown in Table 1. Many of these functions can be performed by a single computer or a master control computer directing the activities of many distributed minicomputer or microprocessor units. No installations have combined relaying with all of the control and data acquisition functions; however, most installations have not included the protection functions and have concentrated on data acquisition.

TABLE 1

Substation Computer Functions

- *Primary Fault Detection
- *Fault Classification
- *Breaker Tripping
- *Fault Location
- *Back-up Fault Detection
- *Bus Bar Protection
- *Transformer Protection
  - -Gas Pressure
  - -Gas Analysis
  - -Moisture Content, etc.
- *Adaptive Relay Settings
- *Adaptive Breaker Control
  - -Breaker Failure(Analysis and Recovery)
  - -Reclosing Control
- *Voltage and Reactive Control
  - -Switching Control in Discrete Steps
- *Load Shedding and Rejection
- *Sectionalizing
- *Load Survey
- *Load Protection
- *Load Distribution
- *Oscillography
  - -Pre-Post Fault Data and Analysis
- *Communications Control
  - -Encoding, Coding, Error Control
- *Synchro Check
- *Data Logging
  - -Analog Metering, Demand Metering
    - MW
    - MVAR
    - Power Factor
    - Voltage
    - Voltage Angle
    - Current
    - Frequency
    - Line Loss and MWH Calculations
- *Transformer Information
- *Breaker and Disconnect Status
- *Relay Status
- *Tap Settings
- *All Other Contact Status
- *Sequence of Events
- *Environment Checks
- *Weather Information
- *Control Room Temperature
- *Temperature of Other Elements
- *Computer Equipment Checks
- *Power Supply Monitor

Many utilities now have SCADA remotes implementing many of the functions in Table 1. As systems evolve using the computer as SCADA remotes, it is very difficult to add additional control functions such as protection. However, if a system evolves to perform protection functions, it is felt that many of the other functions could be implemented in a single control system.

ACTIVE APPROACHES

The active approaches consist of pulse radar and the frequency modulated sweep system. This section discusses these two techniques.

Pulse Radar Systems

As early as the 1940's, engineers were aware of the possible usefulness of applying radar techniques as fault location systems for cables and transmission lines. Construction efforts on these original systems were primarily limited to those employing pulse radar techniques, with the frequency-modulated radar approach, where the target range was related to a frequency measurement the earlier fault location work was principally concerned with the measurement of a voltage amplitude related to the received frequency.

The pulse systems have had an interesting history of being rediscovered, while frequency-modulated systems have not been discussed since the 1940's. In the late 50's and early 60's, the pulse system made a reappearance as a new technique in fault location systems. Today it has taken its place along with other systems as a useful tool in fault location.

The simplest pulse radar system would consist of a transmitter, a single stationary reflecting target, a receiver to detect the reflected signal, and an antenna. The pulse radar system transmits a pulse of short duration and then remains idle for a time period long enough to allow the transmitted pulse to reach its target and be reflected. The time required for the pulse to travel to the target and be reflected is directly proportional to the distance to the target. The distance can be found using the following equation:

$$d = \frac{\nu T}{2} \qquad (1)$$

where

d = distance to target;
ν = speed of wave propagation;
T = time from transmission of pulse to the reception of reflected pulse.

If an ideal environment existed such that the radar system could transmit a square pulse of length τ and after T seconds receive a reflected pulse still square and unaffected by noise, the accuracy of the system could be unlimited. The sad realization is that these ideal conditions do not exist; therefore, the accuracy of any system is limited. Receiver bandwidth, coupled with noise, plays a large role in just how accurate a system can be made to operate. The error in measurement of a signal can be analyzed by assuming a bandwidth-limited rectangular pulse and noting the effect of noise upon the leading and trailing edges. With a receiver bandwidth of B hertz, the rise and fall time of the pulse becomes $\tau_e = 1/B$ sec. This time is actually the time required for the voltage to increase from $0.1E_s$ to $0.9E_s$. This portion of the rise time is approximately linear and the slope of the wave form near the 50 percent point is given by

$$k_e = \frac{E_s}{\tau_e} = E_s B \text{ volts per second}$$

as shown in Figure 1.

The effect of a small additive noise term E_n will modify the 50 percent crossing point as shown in Figure 2. The portion of the pulse shown in Figure 2 is an enlargement of the circled area in Figure 1.

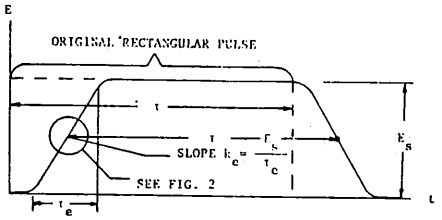


Figure 1

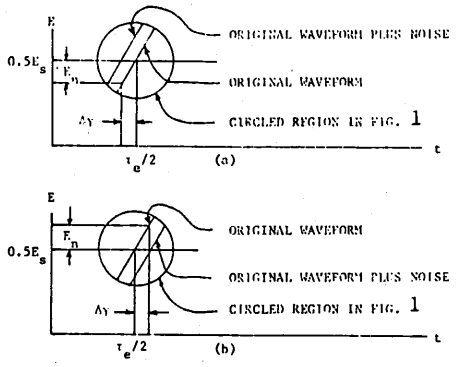


Figure 2

Additive Noise Effects at 50 Percent Point
(a) In-phase Noise
(b) Out-of-phase

From this figure, the following expressions are obtained:

$$\frac{E_s}{2} + E_n = \left(\frac{\tau_e}{2} + \Delta_\gamma\right) k_e \text{ out-of-phase noise ;} \qquad (2)$$

$$\frac{E_s}{2} - E_n = \left(\frac{\tau_e}{2} - \Delta_\gamma\right) k_e \text{ in-phase noise.} \qquad (3)$$

Solving for $\Delta_\gamma = E_n/k_e$ for either in-phase or out-of-phase noise.

Assuming the noise is Gaussian and the pulse width is greater than 1/8 the noise will be dependent from leading edge to trailing edge. These assumptions allow the standard deviation to be written as:

$$\sigma = \frac{\Delta_Y}{\sqrt{2}} = \frac{1}{\sqrt{2B}\,\frac{E_s}{E_n}} = \frac{1}{2B\sqrt{\frac{S}{n}}} \qquad (4)$$

It should be noted that in the above expression, σ is a function of the signal to noise ratio and the bandwidth, but the signal-to-noise ratio is also a function of the bandwidth. The larger the bandwidth, the smaller the signal-to-noise ratio. This results in σ being improved only by the square root of the bandwidth rather than directly as the equation would first indicate.

Frequency-Modulated Radar Systems 31

The frequency-modulated radar system developed at the University of Missouri-Columbia is similar to the pulse system in that it also requires a transmitter, receiver, antenna, and a reflecting target. Again, the simple case of a stationary target will be considered. The frequency-modulated radar system transmits a continuous wave form. The case to be considered here employs a sawtooth wave form as the modulating signal. This provides a transmitted signal that varies linearly with time for a given time interval, then repeats. This signal reaches a reflecting target and returns to the antenna. The signals present at the antenna are shown in Figure 3. The frequency difference of the two wave forms shown in Figure 3 is a constant frequency in the time interval $n\tau + T$ to $(n+1)\tau$ for $n = 1,2,\ldots,N$. T is the time required for the wave to travel from the transmitter to the target and back, and τ is the sweep duration. This constant frequency is directly proportional to the distance to the target, and is given by the equation:

$$d = \frac{\nu T}{2} = \frac{\nu\,\tau\,\delta\,F}{2\Delta F} \qquad (5)$$

d = distance to fault
ν = velocity of wave propagation
T = time required for wave to travel to and from fault
τ = sweep duration
δF = difference frequency
DF = sweep frequency

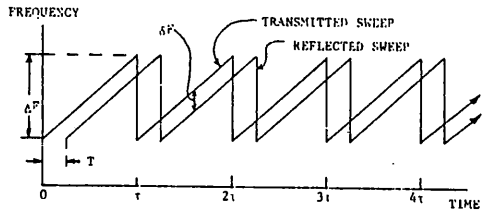


Figure 3

Frequencies Present on Radar Antenna as a Function of Time

It is now desirable to estimate the accuracy with which δF can be measured. As in the pulse radar system, there ia an inaccuracy in the time measurement to and from the reflecting object. The frequency δF and time T are related in this manner:

$$\delta F = \frac{T}{\tau}\,\Delta F \qquad (6)$$

It can easily be seen an error in the measurement of T results in an error in δF of the form

$$\sigma F = \frac{\sigma}{\tau}\,\Delta F \qquad (7)$$

Skolnik gives this expression for the standard deviation in the measurement of T for a single frequency-modulated sweep.

$$\sigma = \frac{3}{\pi\Delta F\,(2E/N_o)^{\frac{1}{2}}} \qquad (8)$$

Using Barton's expression

$$\frac{E}{N_o} = \tau_o\ f\tau\Delta F\frac{S}{N} \qquad (9)$$

in equation 8 results in:

$$\sigma = \frac{\sqrt{3}}{\pi\Delta F(2t_o f\tau\Delta F\ S/N)} \qquad (10)$$

The terms t_o and f are the observation time and the frequency of the sweep repitition. This product, for a single sweep observed for a length of time equal to the sweep length, equals 1. Therefore, in equation 10

$$t_o f = 1$$

resulting in

$$\sigma = \frac{\sqrt{3}}{\pi\Delta F\ (2\Delta F\tau\ S/N)^{\frac{1}{2}}} \qquad (11)$$

(This expression is correct for S/N>1 and $\Delta F\tau$ large.)

Comparison of Pulse and Frequency-Modulated Radar

At this point, it is interesting to make a comparison of the pulse radar and the frequency-modulated radar standard deviation in the time measurement. To make a more meaningful comparison, these restrictions will be placed on the equations for the standard deviations. The energy contained in the pulse and the sweep will be equal, also the bandwidth of the pulse system will be equal to the frequency sweep of the frequency-modulated system. These restrictions make the signal-to-noise ratio equal and ΔF equal B. Now, taking the ratio of the standard deviation of the pulse systems given by equation 4 to that of the frequency-modulated system given in equation 11

with restrictions

$\Delta F = B$

$$\frac{S}{N_p} = \frac{S}{N_F}$$

It is found that

$$\frac{\sigma_p}{\sigma_{Ft}} = \frac{\pi}{\sqrt{6}}\,(B\tau)^{\frac{1}{2}} \qquad (12)$$

This equation shows that for a Bτ product greater than one, the frequency-modulated system will produce more accurate results. For a moving target, the pulse method would measure the speed of the target more accurately as described by Skolnik.

A frequency-modulated radar system when applied to a transmission line possesses the same advantages as a pulse system. The frequency sweep applied to the same line as a pulse will undergo the same frequency attenuation that tends to distort the pulse. This attenuation results in a quite different effect upon the frequency-modulated system. For a linear sweep, the voltage waveform of δF takes the form

$$e = E \sin 2\pi\delta Ft \qquad (13)$$

Where, "E" depends on the amplitude of the transmitted and reflected waveforms, and δF is a constant frequency determined by the delay time between the transmitted and reflected wave, the effects of attenuation of the frequencies within the sweep tends only to affect the amplitude of the difference frequency. The desired information pertaining to the location of the fault is contained in the frequency, not the amplitude of the wave form given in equation 13. This condition gives a frequency-modulated system a definite advantage over the pulse system.

A comparison of the two systems can best be given by an example. First it is assumed that existing carrier systems on the line limit the bandwidth to 50 kH_z.

$$B = 50\ kH_z$$

Next, a 15 kH_z sweep is selected for the frequency-modulated system in such a manner that it does not interfere with the existing carriers.

$$\Delta F = 15\ kH_z$$

The sweep length of the frequency-modulated system is set at 8 msec.

$$\tau = 8 \times 10^{3}$$

These values when substituted into equations 4 and 11 provide

$$\sigma = 10^{5} / \sqrt{S/N} \qquad (14)$$

for the pulse system and

$$\sigma = .235 \times 10^{5} / \sqrt{S/N} \qquad (15)$$

for the frequency-modulated system. The signal-to-noise ratio in equations 15 and 16 is a function of the bandwidth. The pulse system has a bandwidth of 50 kHz or the total available range. The frequency-modulated system has a bandwidth of only 15 kHz or the width of the sweep. This results in the signal-to-noise ratio of the pulse being less than that of the frequency-modulated system. For simplification of comparison, it will be assumed that the signal-to-noise ratios are equal. Making this assumption still gives the frequency-modulated system a smaller error in the measurement(1 as compared to 0.235). This result of a smaller error in measurement, coupled with the effects of attenuation on the two systems, indicates that the frequency-modulated system can operate better in the environment associated with fault location on transmission lines. A typical voltage level for noise can be obtained and noise power calculated.

$$\text{Noise Voltage} = 0.01 \text{ volts} = N_v$$

A typical value of characteristic impedance for a transmission line is 300 Ω. The noise power can be calculated from the equation:

$$N = \frac{(N_v)^2}{Z_o}\ \Delta F \qquad (16)$$

Using the above values to calculate the noise power results in the value of N = .02 watts. It is now necessary to determine the signal power. Assume the frequency-modulated system provides 100 watts to the coupling-decoupling network. A 12 db loss is assumed through the coupling-decoupling network. Assume the attenuation at 50 kHz is 0.065 db per mile. A value of 0.05 db per mile is used assuming thw sweep is below 35 kHz. A line of 200 miles is assumed and a fault placed at the 200 miles point allowing for maximum attenuation. The total line attenuation then becomes

$$2L_a = 2(0.05 \times 200) = 200 \text{ db}$$

This is an attenuation of 10 db as the signal travels to the fault and 10 db as the reflected signal returns from the fault. The total attenuation to the signal prior to entering the decoupling portion of the couplin-decoupling network is the line attenuation plus the coupling attenuation.

$$A_T = C_a + 2L_a = 12 + 20 = 32 \text{ db.}$$

The signal power at this point can be determined from the equation.

$$C_a + 2L_a = 10 \log \frac{P_{in}}{P_{out}}$$

This gives a signal power of 0.063 watts.

$$S = 0.063 \text{ watts.}$$

Since the signal and noise must both pass through the decoupling network, the signal-to-noise ratio will not change from a value that can now be determined.

$$\frac{S}{N} = \frac{0.063}{.02} = 3.15$$

From equations 7 and 11, the uncertainty in the measurement of δF is found to be

$$\sigma F = 2.5 \text{ cycles.}$$

The uncertainty of 2.5 cycles in the frequency measurement corresponds to an uncertainty of approximately 0.1 miles or 530 feet for a 200 mile line.

Prototype Hardware 31

A prototype fault locator system utilizing the frequency-modulated sweep technique was built and the prototype system was tested on an artificial transmission line and in field tests on utility lines. The laboratory test results showed that errors between measured and theoretically calculated distances as low as 0.286% can be achieved. When the prototype system was tested on a power transmission line, the results compared favorably with data obtained in the laboratory. At that time, the prototype design was not, however, optimized to operate in the noisy and lossy conditions which exist on a real line.

The prototype system consists of the following functional parts:

1. Ramp Generator;
2. Voltage Controlled Oscillator (VCO);
3. Transmitter (power amp.);
4. Detector;
5. Gating, window, compensator, etc.

A block diagram of the Ramp Generator is shown in Figure 4.

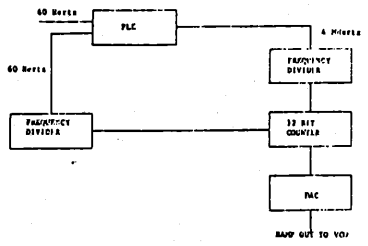


Figure 4

Ramp Generator

The phase lock loop oscillator provides a 4 MHz signal which is frequency divided to provide the clock input to the 12-bit counter, the output which is converted to a ramp by a ditial-to-analog converter. The most significant bit of the counter is further divided in frequency to provide feedback to the phase locked loop. This signal is compared with the 60 Hz signal from the line to keep the phase locked loop (PLL) oscillator synchronized with the line frequency.

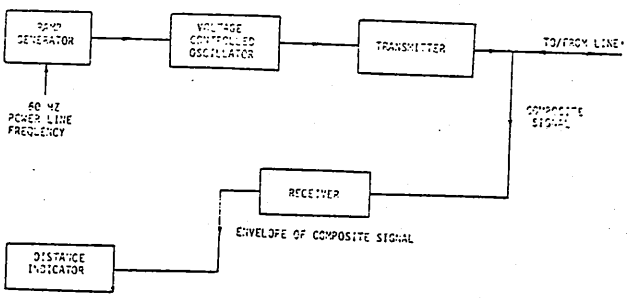


Figure 5

Basic FM Transmitter Configuration

The voltage controlled oscillator used during the first two field tests was an IC VCO chip (Signetics 566). Later tests used the HP3311 function generator which is a separate unit.

The transmitter is a two stage, class A, power amplifier transformer coupled to the line coupling circuit.

The detector circuit consists of a composite filter, a multiplier (squaring ckt), and a low pass filter. During the first two field tests, the composite filter was a 10 kHz HP filter to eliminate 60 cycles from entering the multiplier. For the later field tests, it was a Band Pass filter centered at 134.17 kHz and with cutoff frequencies of 120 kHz and 150 kHz.

During the first two field tests, the output of the multiplier was fed into a 5 kHz low pass filter and the recorded difference frequency was taken from the output of the filter. During later tests, a 180 Hz high pass filter was inserted after the low pass filter.

Field Tests [7]

The FM sweep system has been tested in the field on both de-energized and energized transmission lines under a variety of conditions. After testing, the prototype system has been modified to improve both the ease of operation in the field and the accuracy with which frequency measurements may be made. Figure 5 shows the basic configuration of the system used for field tests. The main objective of the previous field tests has been to determine the line attenuation propagation and reflection characteristics at various frequencies and to design the transmitter and receiver to improve the method of analyzing this difference frequency signal for easier field analysis.

The first tests of the original system were made on an unenergized line with a variety of termination conditions at the end of the line. Later tests were made with a modified system on an energized line. The signal reflection for the energized tests was obtained from the end of the line with a relatively poor reflection coefficient of -1. The FM system was coupled to the B phase of the line through a capacitor-coupled potential device. The results of the field tests are shown in Table 2.

In the table, part of the data is presented as a mean line distance which is the average calculated from the distances obtained from the set described by the variations of ΔF and τ. The standard deviation is also presented for each test with the % error between the actual line length and the mean measured line length calculated from the difference frequency.

The first field test was performed on an unenergized 230 KV, 75 mile line (Wray to Story, Colorado) on the Tri-State Transmission and Generation Association System. Tests were made with the line open and grounded at the far end and with a line-to-ground fault at approximately 1/3 of the line distance. The FM system was directly coupled through a 300 Ω lead to the B phase of the transmission line. An error of .167% was recorded for the full line length and an error of 1.764% was observed for the fault at 1/3 of the total line length.

The primary purpose of this test was to determine attenuation and the signal strength required at various frequencies to obtain a reasonable reflected signal. The frequency range was 15 kHz with a sweep length of 8.33 milliseconds. These tests were performed at 10-25 kHz, 45-60 kHz and 85-100 kHz. Good test results were obtained and less than 4 db attenuation was observed in the 10-25 kHz.

It was determined that a good signal could be received in the range of .1 KW - 1 KW of transmitted power.

The second field test was performed on the Missouri Public Service 60 KV unenergized line, between Blue Springs and Raytown, Missouri. The line is 12.25 miles long, and tests were performed when the line was grounded open and terminated with a resistance. The sweep length was 8.33 milliseconds and frequency range used was 92.082 to 195.085 kHz. The FM system was directly coupled with a 300 Ω line to the B phase. As can be seen from Table 2, generally better results were obtained than in the first field test. The error between the line distance and the mean measured distance is .247%. The results observed were better even though the signal contained more reflections from slightly dissimilar line sections and from an energized line paralleling the line under test for part of the distance. As a result of the experience gained on the first field test, the system was re-designed and configured for easier operation in the field.

The third field test was performed on Union Electric's 345 KV line between Overton and Montgomery City, Missouri. The line was energized and had several carrier frequencies present. The FM sweep system was coupled through the coupling device for their 140 kHz carrier signal. The line was 66.00 miles long (with sag) and the frequency range was 120.57 kHz to 150.19 kHz with a sweep length of 16.68 milliseconds. Line traps were located at each end of the line which very nearly matched the line at the carrier frequency. Due to the wave traps the reflection coefficient is quite low and thus produces a very small reflected signal. In order to detect the reflected signal, unwanted signals were filtered with a band pass filter. The distance to the end of the line section was determined with a .0508% error between the actual line length and the mean measured line length.

Further tests have been performed on a 2.249 mile cable located at the University of Missouri-Columbia. Several different frequency ranges have been used at a sweep length of 16.68 milliseconds. Tests have been made for open, shorted and various impedance terminations at the end of the line.

Sources of Error

It is anticipated that the FM system can be used to locate faults on overhead transmission lines within 1 tower span. The tests, described in this report, were not performed to achieve the greatest possible accuracy,

Table 2

LOCATION	TEST CONDITION	ACTUAL LINE LENGTH	MEAN MEASURED LINE LENGTH	STANDARD DEVIATION	Δ% BETWEEN ACTUAL AND MEASURED	APPROX. # OF CYCLES PER SWEEP	METHOD OF MEASUREMENT
Wray, Colo.	De-energized full length fault, phase to ground	75.945	75.598	0.488	-0.457	12.457	Count # of cycles per sweep.
	Fault at 1/3 of phase line to ground	31.295	30.350	0.068	-3.019	4.934	
	De-energized full length short phase to ground	75.945	75.824	0.642	-0.167	12.253	Spectrum Analyzer
	Fault at 1/3 phase to ground	31.295	30.743	0.210	-1.764	4.999	
Blue Springs, Missouri	De-energized full length i. fault phase to ground ii. open iii. 140Ω termination	12.250	12.220	0.403	-0.247	13.681	Spectrum Analyzer
Overton, Missouri	Energized full length Line trap into a substation	661990	66.956	1.452	-.0508	21.428	Spectrum Analyzer
Coaxial Cable UMC EE Lab	De-energized full length	2.249	2.280	0.099	1.398	3.003	Spectrum Analyzer
	Open and short circuit						

but were intended to provide necessary information concerning signal propagation and reflection. This information will be incorporated into the receiver design to improve the locating accuracy. For the tests previously performed, it is very difficult to accurately determine the actual line length. The line sag was estimated for each line and could easily introduce up to 1% error. The survey of the linear distance sometimes is in error by as much as 1%. Additional sources of error can be produced by non-linearities of the transmitter and the method used to determine the difference frequency. The system can be calibrated as a function of the detected line length prior to a fault to compensate for environmental changes in sag.

A general description of the principles involved in the FM radar, as well as a description of a prototype unit at the University of Missouri-Columbia, was presented. Results taken on three field tests on both unenergized and energized transmission lines have been described.

The primary method of analyzing the difference frequency data to determine the fault distance has been to display the composite and/or difference frequency on an oscilloscope and to compute the difference frequency by counting cycles. This technique could be quite easily automated because the signal-to-noise ratio in the power line application is usually high enough that the frequency is unambiguous. When the signal-to-noise ratio is low, then pulse compression processing of the return signal should be applied which would greatly increase the complexity of the system. A further limitation of the operation of the FM fault locator as described here is that very short lines(or lines with very close-in faults) are difficult to deal with because less than one cycle of the difference frequency is produced for analysis. This problem can be offset in part by using large values of Δf. With Δf = 250 kHz and v_p = 186000 mi/sec., the fault distance should be greater than about 1/3 mile for reliable operation.

TRANSIENT METHODS

The sudden occurrence of a fault on a power transmission line causes a propagaion of traveling waves toward both ends of a transmission line. When the traveling waves reach the ends of a transmission line, they are reflected back to the fault point. The line resistance and other losses tend to attenuate and distort the impinging wavefronts. The reflection caused by a fault produce a high frequency transient that can be recorded at the end of the line. The high frequency transient decays exponentially and lasts for a period of time which is dependent upon the parameters of the line.

While the presence of a high frequency transient superimposed on the 60 Hz fault voltage and current waveforms must be removed for most of the transmission line protection methods presented in Chapter IV, it is possible to use the high frequency transient to detect and locate faults.

Several techniques have been proposed to use the transient information to detect faults. This section describes the following proposed techniques:

1. High Frequency Transient Methods
2. Initial Transient Methods
   a) Discontinuity Detection Methods
   b) Traveling Wave Discriminant
   c) Current Differential Carrier

High Frequency Transient Fault Detection

It has been demonstrated that high frequencies with a predominant component in the range of 400 Hz to 10 kHz exists for about one cycle after the inception of a fault.

The frequency of the high frequency transient is inversely proportional to the distance to the fault and is dependent on the type of fault. The magnitude of the high frequency transient is dependent on the angle of the 60 Hz voltage at the inception of the fault (12).

A computer program was developed at the University of Missouri-Columbia to calculate the fault transient waveform. The computer program was developed to plot the voltage and current waveforms of the reference phase for all types of faults. Figures 6 and 7 show voltage and current waveforms for a typical system as recorded at the sending end of the line.

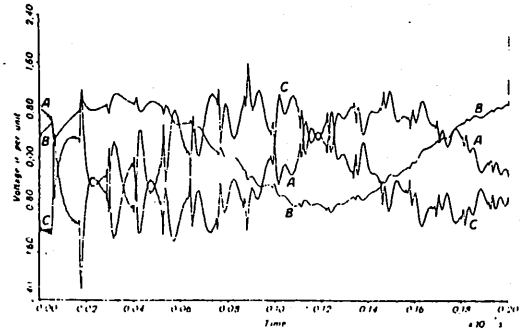


Figure 6

Voltage Waveform for a Three-Phase Fault at 160,930 Km(100 Miles), 120°

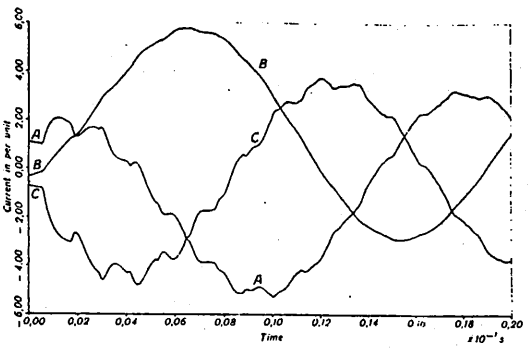


Figure 7

Current Waveform for a Three-Phase Fault at 160,930 Km(100 Miles),120°

A transient network analyzer using lumped parameter pi sections has accurately duplicated waveforms with high frequency components taken from oscillograms of faults on actual power systems. Frequencies obtained with the TNA also compared closely with those predicted by calculations. For three-phase faults located from 50 to 200 miles away on a simulated line, the TNA produced frequencies ranging from 1135 to 324 Hz. For line-to-line faults over the same distance, frequencies ranged from 1110 to 341 Hz. For one-line-to-ground faults, the frequencies ranged from 975 to 312 Hz.

A frequency detector was built to measure the high frequency transient (10). The frequency detector consists of a bandpass filter to attenuate the power system frequency and to prevent spurious triggering of the peak detector, which generates a 500 ns. pulse at each peak, and logic which counts the peaks and checks the number of peaks in a specified interval to insure that the frequencies are in the range to indicate a fault.

The main function of the frequency detector in computer relaying would be that of fault detection and location. When the frequency detector indicates the presence of a fault, the computer goes into the fault mode of operation and analyzes, 60 Hz voltage, current, and phase angle to determine the type of fault and the faulted line. The frequency of the high frequency transient is used to determine the zone the fault is located in. After the fault has been cleared, the computer makes an accurate calculation of the fault location from the frequency of the high frequency transient.

These types of techniques free the computer from continually sampling voltage and current waveforms to determine whether a fault exists. When a fault is detected, the computer is signaled to go into the fault mode, thus freeing the computer for other functions during the 99.9% of the time that the normal conditions exists.

Description of the Substation Computer Control System

The substation control unit is comprised of three sections as shown in figure 8. The line interface units are located on each phase of each line in the substation and the fault detector interface is located on each phase of each bus in a substation.

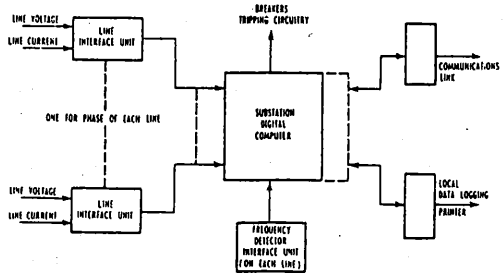


Figure 8
Direct Digital Controlled Substation System

The special interface units allow the digital computer to be a mini-computer specially designed to handle the type of data and make the necessary calculations pertinent to substation operation. The computer can be either hardwired or stored program control depending upon the degree of sophistication and flexibility desired. The modular design allows the flexibility to attain the degree of control desired for the various size substations for both transmission and distribution systems.

The substation computer coordinates and reports the functions of the substation with the central control system. Microwave communication facilities may transmit data to and from the substation site. In addition, a local data logging printer prints a complete log of substation operation at the substation site.

Frequency Detector Interface Unit

The presence of the high-frequency transient indicates the possible existence of fault conditions. Therefore if the high-frequency transient can be detected then a signal can be given to the substation digital computer to go into the fault mode. Furthermore, if the frequency can be measured, the location of the fault can be calculated. When a high-frequency transient occurs the frequency detector obtains and stores information necessary to calculate frequency and notifies the digital computer of the possible existence of a fault. The computer then samples the output of the line interface units located on each phase of each line. The computer obtains readings of voltage, current and phase from the line interface units to verify the existence of a fault and determine which phases are affected by the fault. The computer then starts the fault clearing procedures to deenergize the faulted line. This method of detection relieves the digital computer from continuously sampling each phase of each line to determine whether fault conditions exist. Figure 9 shows a block diagram of the frequency detector interface unit.

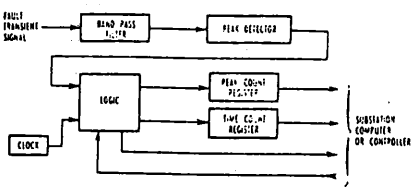


Figure 9
Frequency Detector Interface Unit Block Diagram

The filter shown in figure 9 is used to suppress the basic 60 Hz fault waveform and to allow the high frequency transient to pass through to the peak detector. The peak detector senses the positive peaks and provides a switched output and a peak value output. The peak value output is compared against a reference voltage which is related to the minimum expected high frequency transient amplitude. The pulse output of the peak detector drives the logic circuitry.

The logic circuitry performs two functions:

1.) Detect whether the pulses from the peak detector are in proper frequency range.

2.) Provide sufficient information to the digital computer to calculate the frequency of the high-frequency transient.

Line Interface Unit

Figure 10 shows the basic design and illustrates the operation of the line interface units.

The purpose of the line interface circuit is to make available to the digital computer peak voltage, peak current and phase angle. A zero crossing detector detects the voltage zero and outputs a pulse which starts a voltage time counter. When the counter has counted up to 90° the peak value of voltage is held in a sample and hold circuit and is converted to a digital number.

The current zero point is detected by another zero crossing detector which stores the value of the voltage time counter at that time into a register. The register then has the phase angle in digital form for either leading or lagging phase angle. After 90° on the current waveform the peak current is held in another sample and hold circuit. The line interface unit has been constructed utilizing integrated circuits.

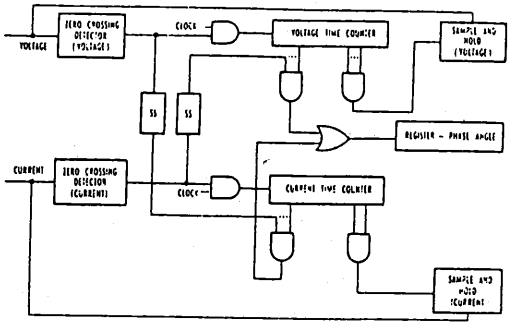


Figure 10

Line Interface Unit

When the computer is signaled by the frequency detector that there is a fault, the computer then reads the peak voltage, peak current and phase angle for each phase of each line. The faulted line is determined from comparing these three values with previously determined normal values. The computer has stored in it normal operation values, below which indicates normal operation. The readings are compared with these reference values to determine whether abnormal conditions exist. The computer has the ability to change the reference setting by command from central point, whereas a relay setting must be manually set. From the detector peak count and time count registers the computer calculates the frequency of the fault transient and hence the distance to the fault. If the fault is in the proper zone the breaker tripping circuitry is signaled to open the faulted line.

Initial Transient Methods - Basic Premises

Several of the approaches to ultra-high speed relaying currently being developed depend upon detecting the presence of a fault within the protected region by identifying the initial onset of the traveling wave which proceeds both ways along the line from a suddenly occurring fault. These methods try to use the perturbations of voltage and/or current as soon as they can be positively recognized at the relay location. They differ in this regard from fast impedance-calculating algorithms which try to ignore or "see through" the transient to identify as quickly as possible the new (sinusoidal) steady state values of voltage and current, from which the impedance "seen" at the relay point can be calculated.

Stripped to their simplest models, the transient methods all depend on the well known solutions, due to D'Alembert, for the lossless line equations:

Equations

$$\frac{-\delta v}{\partial x} = L \frac{di}{dt} \qquad (17)$$

$$\frac{-\delta i}{\partial x} = C \frac{dv}{dt} \qquad (18)$$

Solutions

$$i(x,t) = \phi^{+}(x-at) + \phi^{-}(x+at) \qquad (19)$$

$$v(x,t) = Z\phi^{+}(x-at) - Z\phi^{-}(x+at) \qquad (20)$$

where

L=series inductance per unit length
C=shunt capacitance per unit length
$Z=\sqrt{L/C}$ = line surge impedance
$a = \frac{1}{\sqrt{LC}}$ = velocity of propagation

The functions of ϕ^{+} and ϕ^{-} represent traveling waves which move in the positive and negative x directions, respectively. Their exact form depends upon boundary conditions in time and space along the line. None of the traveling wave relay methods requires detailed knowledge of the shape of the functions ϕ^{+} and ϕ^{-}. Such a requirement would be impractical because of the highly varied and irregular waveforms observed on real lines (or in realistic simulations) under fault conditions. The three methods described here all depend on certain invariant aspects of the transient phenomena following a fault onset. They are identified in Table 3, which also gives their principles of fault detection.

Relay	Developer (s)	Basis for Fault Detection
Traveling-wave Discriminant (TWD)	Boeing Company and Bonneville Power Administration (H.W. Dommel and J. Michels)	Calculated function of deviation between received and reference current and voltage which is invariant with respect to fault initiation angle and line termination.
Current Differential Carrier (CDC)	Tokyo Electric, Hitachi, Ltd. Mitsubishi Electric (T. Takagi, et. al.)	Differences in current and voltage waveforms at two ends of protected line. The waveforms will be invariant if there is no fault present.
RALDA	ASEA (Sweden) (M. Chamia and S. Libermann) Bonneville Power Administration (M. Lee and J. Esztergalyos)	Comparisons of instantaneous deviation of current and voltage from un-faulted values with pre-determined threshold levels for Δi and Δv. Depends on premise that currents and voltages themselves are (almost) invariant.

Table 3

Traveling Wave Discriminant (TWD) Relay

Dommel and Michels described the mathematical foundations for the TWD relay in a recent paper (73). They have devised a traveling-wave discriminant function

$$D = (V-ZI)^2 + \frac{1}{\omega^2}\left(\frac{dv}{dt} - Z\frac{dI}{dt}\right)^2 \qquad (21)$$

in which v = the initial change in voltage associated with a suddenly occurring fault.
and I = the initial change in current associated with a suddenly occurring fault.

Figure 11 shows the simplest case of a single line-to-ground fault and makes no attempt to illustrate detailed waveforms.

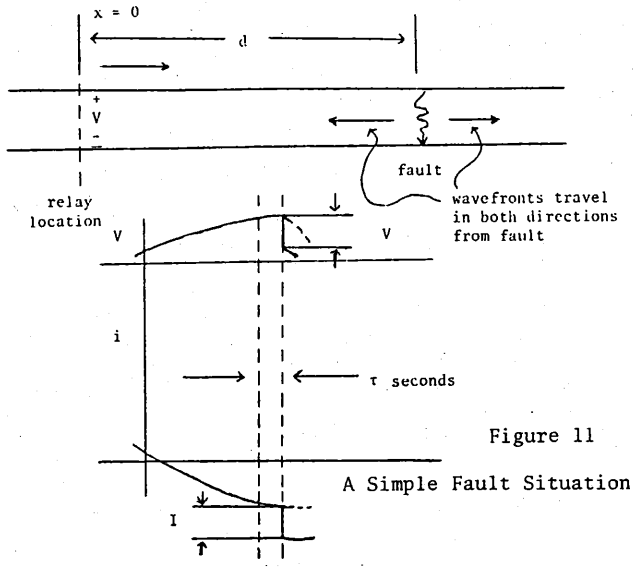


Figure 11

A Simple Fault Situation

Dommel and Michels have shown that D is invariant with respect to the location of the fault relative to the relay terminals and with respect to the initiation angle at which the fault occurs. Voltage and current changes on the line are related so that D would be (in principle) zero for a fault occurring behind the relay (x<0 in figure 11), thus giving the TWD relay excellent directionality. The validity of the TWD function's invariant properties has been established for other fault types than single-line-to-ground using (α, β, 0) modal components of voltages and currents.

The TWD relay does not yet exist in hardware prototype form. The idea has been tested on a wide variety of simulated fault waveforms using a conveniently available large computer. Its performance was quite satisfactory except in a few cases in which multiple reflections on a short line caused erratic results. The original program was written in FORTRAN.

The Boeing TWD program monitors all three line to ground voltages for deviations of more than .06 per unit from one cycle to the next. When it finds such a deviation, the program calculates the value of D for all three phases and for the zero sequence components. If D exceeds a threshold level for more than three consecutive sample times, a fault is declared to exist and its nature is determined by considerations of which D values are above the threshold. The success of such a relay depends on the appropriate setting of the thresholds for voltage deviation and for the D values. The levels used by Boeing were determined during the course of extensive simulation studies. No explicit threshold setting procedure has been reported. This would, no doubt, have to be subject to adjustment to match actual line characteristics in field testing of a prototype relay.

Bonneville Power Administration has subsequently developed a limited simulation of the TWD relay in assembly language for a minicomputer using 16-bit integer arithmetic. This program, called BTWD, implements adaptive features proposed by Boeing but not included in the original program which allow the relay to follow slow variations in magnitude and frequency without generating fault indications.

Further development of the TWD relay is planned to include adaptation of the BTWD program to accept digitized data from a model transmission line and the continuation of fault simulation studies. No specific plans for installation of a working prototype are currently made. The amount of computing necessary between samples for an on-line TWD relay is approximately 44 multiplications, 36 double-precision (based on a 16-bit process-

or) additions, 24 memory transfers and 6 single precision additions. For the 50 microsecond sampling proposed by Boeing (Final Report on The Conceptual Design of an Ultra High Speed Relay by Boeing D276-10006-1) this would probably require special pipe-lined logic circuitry or a 16-bit microprocessor augmented by a fast external hardware multiplier.

Desirable features of the TWD relay include:

1. Indication of fault occurrence begins 1 to 3 sample intervals after the fault wave arrives at the relay location. This is approximately τ + 100 microseconds, significantly less time than is required by impedance calculating algorithms.
2. Inherent directionality.
3. Insensitivity to DC offset component of fault waveforms, which can be a source of difficulty in impedance calculations.
4. Minimal filtering needed.

Current Differential Carrier Relay (CDC)

Takagi and associates have described a new traveling-wave relay which they call a "d'Alembert relay" that utilizes the fact that the traveling waves of voltage and current on a lossless transmission line having uniformly distributed shunt capacitance and series inductance satisfy the following relationship (78) (79).

$$v_a(x,t-T) + Zi_a(x,t-T) = v_b(x+d,t) + Zi_b(x+d,t) \qquad (22)$$

This equation applies to the line illustrated in figure 12.

T=time of propagation of wave from a to b.
Z=surge impedance of line $= \sqrt{\frac{L}{C}}$.
L=inductance per unit length.
C=capacitance per unit length.

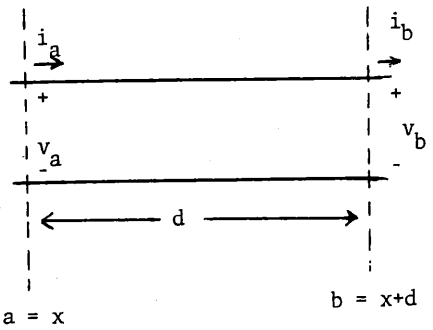


Figure 12 Transmission Line

A difference function which would have zero value if equation (22) were exactly satisified may easily be created and tested against a threshold value to identify a fault occurring within the protected zone (Between a and b). Such a function is given in equation (23).

$$I = i_a(x,t-T) - i_b(x+d,t) + \frac{1}{Z}\{v_a(x,t-T) - v_b(x+d,t)\} \qquad (23)$$

If $|I|>\xi$ (a specific threshold value) an internal fault exists; if $|I|<\xi$, no internal fault exists.

It is necessary to provide a data communication link between ends of the protected line so that the necessary current and voltage values can be brought together for calculating and testing the value of I. The new relay differs from previous current differential carrier relays by using voltage and line surge impedance as well as current in a characteristic function which is invariant with respect to the location of the fault within the protected zone and to the detailed shape of the traveling waves. Equation (23) applies directly to a single phase line. If one considers the mutual coupling between phases of a three phase line, equation (23) does not apply, since it is derived from the single-line wave equation (equation 17 and 18) which does not include terms representing the dependence of the voltage along one line on the current in the other lines. This complication can be handled by transforming the phase voltages and currents into their modal components (α,β,o, or Clarke components), which are not mutually coupled to each other. The function I can be tested for each modal component. In general, the surge impedance and propagation time are different for the different modes. Although the modal decomposition eliminates mutual coupling and permits "one-to-one" waveform comparison, a specific fault may be reflected in more than one mode. It is therefore necessary to reconvert the modal difference functions to phase quantities in order to interpret the nature of faults which may occur. Having established this theoretical rationale, Takagi and co-workers reject as practically unfeasible the actual modal implementation of their relay and apply equation (23) to phase quantities after all. Simulation studies indicate that a threshold can be chosen for (I) which successfully differentiates between fault produced wave-forms on faulted and unfaulted phases.

The new CDC relay is subject to several possible sources of error which have been studied through digital simulation and using a transient network analyzer. These error sources and their assessment or resolution are listed below.

Error Source	Countermeasure
Mutual coupling between lines which leads to spurious indications of I.	Theory: Carry out difference measurements in modal domain. Practice: Use phase quantities and set threshold above spurious signal levels.
Error in T value (Propagation time).	Serious problem which is alleviated by low-pass filtering of I signal.
Error in Z (surge impedance).	Less serious than T error-can be ignored in practice.
Resistive losses in line (not included in basic equations).	Practical resistance values cause no significant errors.
Frequency dependence of line parameters (primarily resistance).	Improves CDC relay performance by tending to filter out high frequencies.
Different T for different protected line lengths.	Use software (interpolation) to create correct T for a given line.

More extensive simulation studies using a microprocessor realization of the relay in conjunction with a special digital simulator are planned, as is field testing in an actual power system.

ASEA Transient Discontinuity Relay

The ASEA "RALDA" relay has been installed in the Bonneville Power Administration 500 kV system since April 1976. Chamia and Liberman have described the operating principles, the overall relay system design, and laboratory tests of the ASEA relay. (84). Yee and Esztergalyos have reported on one year of field experience with the relay on the BPA system. (83).

The ASEA relay senses the initial disturbance of voltage and current of each phase which may be involved in a fault as the traveling-wave created by the fault initially reaches the relay location. It may be shown that for a protected zone between two such relays, internal faults will cause voltage and current deviations ($\Delta v, \Delta i$) from unfaulted values which are opposite in sign (to each other) at both relays. Faults outside the protected zone will cause Δv and Δi to be opposite in sign at one relay but of the same sign at the other. (84) Considering the diagram of Figure (13), we may define the

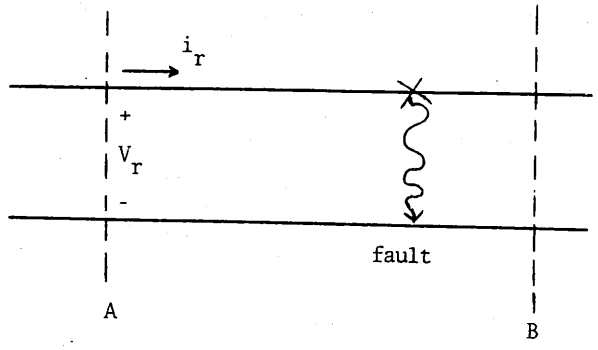


Figure 13

voltage and current at location γ to be:

$$v_r(t) = v_{rn} + \Delta v_r \qquad (25)$$

$$i_r(t) = i_{rn} + \Delta i_r \qquad (26)$$

Where: subscript n denotes normal or un-faulted values.

We can further consider that the disturbances caused by the fault are composed of transient and steady-state portions.

$$v_r(t) = v_{rn} + \Delta v_{rt} + \Delta v_{rs} \qquad (27)$$

$$i_r(t) = i_{rn} + \Delta i_{rt} + \Delta i_{rs} \qquad (28)$$

Where: t=transient and s=steady-state.

Equations (27) and (28) are most useful in classifying relay types. Impedance-type relays must filter out Δv_{rt} and Δi_{rt} in an effort to determine the faulted steady state values. To do this very rapidly poses major filtering or recognition problems. Some transient relays use all or part of Δv_{rt} and Δi_{rt} as an indication that a fault has occurred; for example, the high-frequency transient relay described earlier in this paper. Recognition of the desired component is probably easier in such a case than for impedance relaying. The RALDA relay has the simplest recognition task of all, however, because it filters out v_{rn} and i_{rn} with low-pass filters. Once the normal steady-state frequency is eliminated, any signal appearing in the filter output is indicative of a possible fault. Thresholds are set for both voltage and current to differentiate fault transients from other disturbances caused by switching of power system components and other non-fault transients. The relay depends critically on there being a practically useful range of voltage and current levels in which to place such thresholds and, of course, on their appropriate placement within. The thresholds used are based on steady-state fault calculations for the specific line to be projected. They are set for two modes of relay operation, a direct tripping mode which underreaches the protected line and a transferred-blocking mode which overreaches the protected line. With two such relays "facing" each other two zones are established for each relay. Within its primary forward reach either relay will initiate tripping. Between the end of its primary zone and the remote relay a given relay will initiate tripping unless it receives a blocking signal from the remote relay (indicating the disturbance originated behind the remote relay and hence outside the protected zone).

During the first year of operation the RALDA relay operated in fault modes twenty-eight times. Twenty-four of these events were documented as real internal or external faults and were properly responded to by the relay. Of the four remaining, two cannot be positively explained, but are thought to have resulted from slightly over-sensitive settings on one relay or possibly from transient faults within the protected zone. The final two incidents were improper operations due to a connection error and temperature sensitivity of the trip circuitry of the relay. Redesigned trip modules were installed which gave no further difficulty during the period reported on. (83) The relay also produced 200 system blocking operations during the test period due to microwave communication-link noise and routine power system switching operations.

The RALDA relay has performed well in its field test. It has exhibited virtually perfect reliability in the forward tripping modes and in reverse blocking. It has operated consistently within a 2-6 milliseconds of fault initiation. This system promises, in conjunction with new one-cycle switchgear, to limit total close-in fault times to near one cycle. This unit seems to be clearly the present leader in ultra-high speed relay technology. The elegance and simplicity of its basic principles lend themselves to convenient implementation. Its low power consumption and small ac-circuit burden make it readily applicable in any anticipated field installation.

CHAPTER VI

PROTECTION OF GENERATORS USING DIGITAL COMPUTERS

Last and Stalewsky [2] suggested in 1966 that digital computers may be used in an on-line mode for the protection of power systems. Since then, many digital computer techniques have been developed for the protection of transmission lines, transformers, generators and bus bars. Most of the attention has, however, been focused on the development of and the application of computer techniques for the protection of transmission lines which aspects have been presented in Chapters III and IV. Protection of generators by programmable digital devices which has also received some attention is discussed in this chapter.

Sachdev and Wind [34,36] reported a technique which used a digital computer to detect internal faults of generators. To alleviate some Analog to Digital conversion problems and to reduce cpu time required for computing, the line and neutral side currents were preprocessed. The instantaneous fault current (difference between the line and neutral side current of the faulted phase) was compared with the average of the instantaneous through current immediately after the inception of a fault. Hope, Dash and Malik [67] determined the real and imaginary components of the phasors representing the line and neutral side currents by the Correlation Functions approach. Two different trip criteria were tried. One criterion consists of comparing the magnitude of the difference between the line and neutral side currents of a phase with the sum of the line and the neutral side currents of the phase and tripping when the difference current exceeds a specified percent of the sum current. The second criterion used the dot product of the line and neutral side currents of a phase as the restraining quantity. This approach increases the relay's insensitivity to external faults. A novel technique, proposed by Dash, Malik and Hope [75] detects unsymmetrical faults in a generator by monitoring the second harmonic component in the field current and the direction of the flow of negative sequence power at the terminals of the generator. These authors have taken advantage of the fact that under normal operating conditions and during three phase faults, the field current does not contain any harmonics and their is no exchange of negative sequence power between the generator and the system. During unsymmetrical faults, the field current contains a second harmonic component. In case of external faults, the negative sequence power flows into the generator and, during internal unsymmetrical faults, the negative sequence power flows from the generator to the system. In addition to these developments, some aspects of protecting hydro power plants by using digital devices have been discussed by Sachdev [IEEE Pub. 76CH1057-9REG5, pp. 82-86].

This chapter briefly presents the essential features of the generator differential protection schemes mentioned in the last paragraph. Some of the results obtained by applying these approaches are also included. A few important aspects of digital computer protection of power plants are then discussed. Before presenting the digital approaches, the principle of generator differential protection is briefly outlined.

DIFFERENTIAL PROTECTION OF A GENERATOR

The winding of a generator stator consists of a number of turns of conductors, electrically insulated from but physically embedded in an iron core which is connected directly to ground. Should the insulation between a conductor and the iron core fail, a new current path will be established from the stator winding, through the iron core to ground. The current flowing in the fault loop, which is not directly accessible, can be measured as the difference between the currents entering and leaving each phase of the winding at the neutral and line ends. Differential protection as applied to one phase of a generator is depicted in Fig. 1. During normal operation and external faults, the current, I_1, entering the winding is equal to the current, I_2, leaving the winding if leakage and transducer mismatch are neglected. The fault current, which is proportional to $(I_1 - I_2)$ is generally used to provide operating torque. To avoid undesireable trippings a restraining torque is provided by a suitable combination of the currents I_1 and I_2.

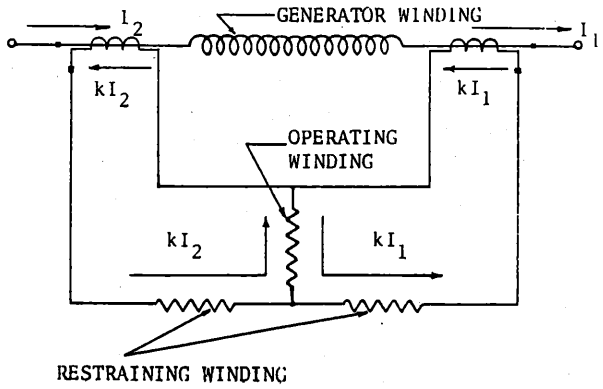


Fig. 1. Connection diagram of one phase of a generator differential protection scheme.

Two distinct approaches have been used in designing digital relays for differential protection of generators. The approach used by Hope and associates [67], extracts the fundamental frequency components of the currents, and from this information decides whether the generator is experiencing a fault. Sachdev and Wind's approach [34,36] compares the instantaneous values of the line and neutral side currents. These methods of differential protection are described in the succeeding sections. Some of the results reported by the authors are also reproduced and discussed.

COMPARISON OF INSTANTANEOUS CURRENTS APPROACH

An analysis of a short circuited generator indicates that the operating and restraining currents are composed of pre and post fault fundamental frequency, exponentially decaying D.C. and high frequency components. Both, the time constants and phase angles of the post fault stator currents depend upon the parameters of the stator and the system. The relay operating current $(I_1 - I_2)$ must rise from zero with a rate restricted by the machine, system and fault parameters; but the restraining current $(I_1 + I_2)$ may not. To facilitate a comparison of the instantaneous operating and restraining currents, Sachdev and Wind [34] suggested that a modified sum current be generated. Figure 2 illustrates the difference, sum and modified sum currents for a

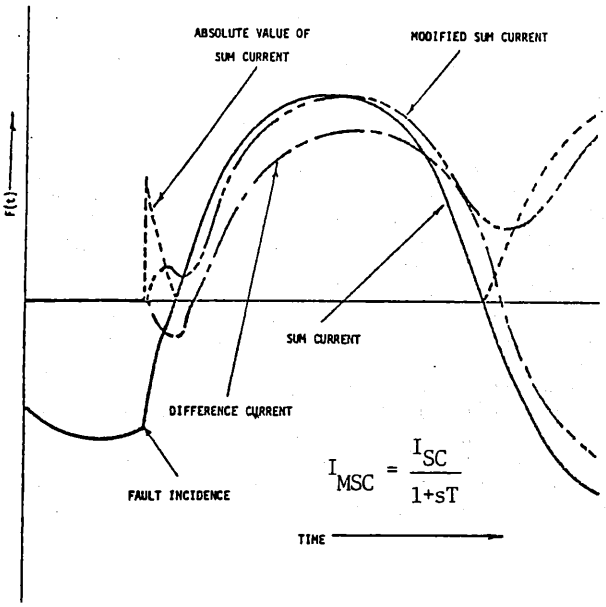


Fig. 2. Sampled and derived functions for a faulted stator as used by the protection scheme.

marginal fault. The algorithm for generating the modified sum current is also shown in this figure. SDS Sigma 2 digital computer was used for the implementation of this relay.

Analog Preprocessors

The digital differential relay described by Sachdev and Wind was developed at the University of Saskatchewan in 1971. Because of the limitations of the equipment available to the authors at that time, the operating and restraining currents (I_1-I_2) and (I_1+I_2) for each generator phase were derived from I_1 and I_2 by using analog circuits of the type shown in Figure 3. The gains of the circuit were adjusted so that the peak amplitudes of the sum and difference currents including the D.C. offsets in the currents would not saturate the analog components and the A/D converters.

Description of the Relay

The organizational structure of the digital differential relay used by Sachdev and Wind is shown in Figure 4. The fault monitor issues read directs to sequentially sample the three difference currents from the analog preprocessor at 15 kHz. These samples are used to update circular tables containing samples of the difference current of each phase. The absolute value of the sample just received is compared to a pre-specified threshold. Should the amplitude of the sample exceed the threshold, the monitor relinquishes control to the phase allocation segment. If the sample is within the threshold limits, the program checks whether the sample was taken as part of the phase allocation routine. If not, the monitor remains active. The difference current sample for the next stator phase is read and the procedure described above is repeated.

On activation by the monitor, the phase allocation segment determines the faulted phase (A, B or C). The monitor could have relinquished control if the difference current was in excess of the threshold in a phase, say phase B. This would activate the allocation segment of the phase B. This segment issues a read direct to

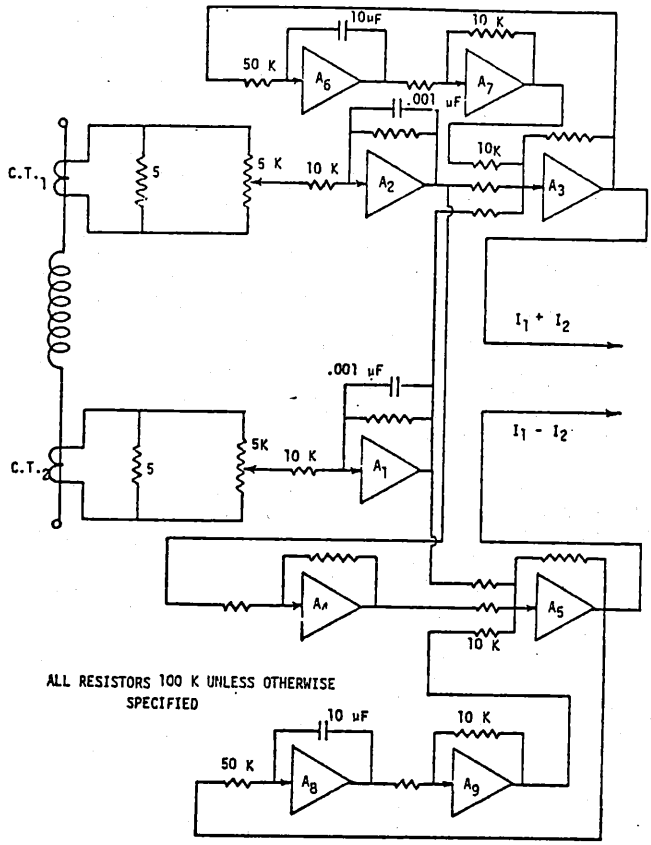


Fig. 3. Schematic diagram of the analog pre-processor.

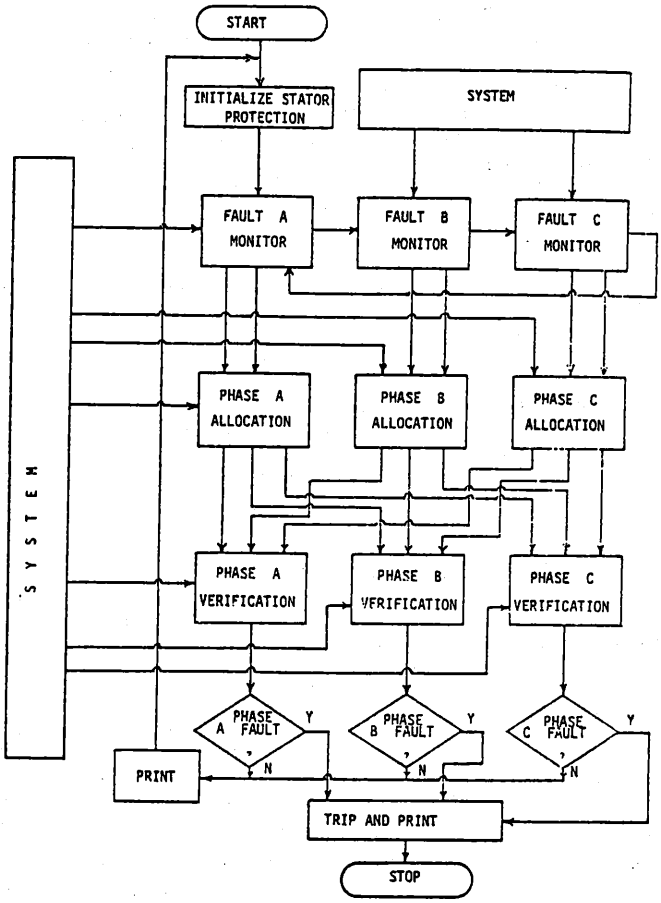


Fig. 4. The logic organization of the proposed digital percentage differential protection scheme.

the A/D convertor to sample the difference current of the next phase, C. The sample is placed in the circular table and its absolute value is calculated. The difference current sample of the next phase, A, is similarly processed. The absolute values of the three samples are compared and the originating phase of the largest current is determined. One pass of the phase allocation segment is now complete. Sequentional sampling continues and the procedure described above is repeated for the next set of samples of the three stator phases. This is continued until the phase allocation passes twice indicate the same phase as probably faulted, say phase A. The program then branches to the appropriate fault verification routine, phase A in this case.

The verification segment decides whether the generator stator is actually faulted or not. One verification segment is provided for each phase. On commencement of verification, the sampling is restricted to the sum and difference currents of the phase selected by the allocation segment. The difference current samples are still stored in the circular tables. Three additional circular storage arrays, one for each phase, are included for the sum currents. A control parameter 'COUNT', is preset and the modified sum current function, 'SUMSAMP', is initialized. The difference current sample, read from the A/D convertor, is placed in the circular store and its absolute value is computed. The absolute value is then multiplied by 128 using an arithmetic left shift of seven bits. Now the value of the last sum current sample is retrieved from the appropriate location in its circular table and the new value of the modified sum current is computed. Next, the sum current sample is read from the A/D convertor.

In the initial few passes, the value of the modified sum current could be small and, to avoid unnecessary computations, a deadband is provided and computations are not allowed unless 'SUMSAMP' exceeds a threshold. Should 'SUMSAMP' be less than the "calculation threshold", the program returns for the next difference current sample. If the threshold is exceeded on any pass, 128 times the absolute value of the last difference current sample is compared with the 'SUMSAMP' times the relay setting. Should the absolute value of the difference current times 128 exceed the relay setting times the 'SUMSAMP', a stator fault is indicated and the counter 'COUNT' is incremented; otherwise the counter is decremented. After 'COUNT' has been either incremented or decremented, it is compared with a positive and a negative threshold value. If the value of the counter is between the two threshold values, the issue is undecided and the program returns for another verification pass. Should 'COUNT' be less than the negative threshold, it is concluded that the allocation and verification routines were triggered by some transient condition. The sum current storage is initialized and the monitor is reinstated. If the 'COUNT', is greater than the positive threshold, it is concluded that the system is experiencing a fault and an appropriate trip command is issued. This procedure was used to reduce the possibility of making incorrect conclusions.

With the inclusion of the calculation threshold feature, a possibility for error was introduced. In-zone faults are conceivable where the contributions to the fault current from the generator and the connected system are in phase and approximately equal in magnitude. For these rare occurrences, the sum current would be small while the difference current would be very large. This condition, if present, could prevent the modified sum current from exceeding the calculation threshold and there by hang up the verification process.

A second counter 'COUNT B', is therefore provided. This counter is incremented in each pass of the allocation and verification segments if the absolute value of the difference current exceeds a back up threshold. After each verification check, 'COUNT B' is compared with an upper limit. The verification sequence concludes that a valid fault condition exists if 'COUNT B' is in excess of the limit.

Testing the Relay

The digital differential relay was tested in the laboratory by applying it to a three phase 5 kVA 220 Volt alternator. This machine has split stator windings which can be either connected in series or in parallel. For these tests, the windings were connected in series as shown in Figure 5. When the generator is operated in this configuration, its rated full load current is 13 amps. A resistance was inserted in the neutral to limit the ground fault currents to about 2 p.u. With the winding terminals all brought out to a front panel, simulation of internal faults was faciliated with minimum risk to personnel and the equipment.

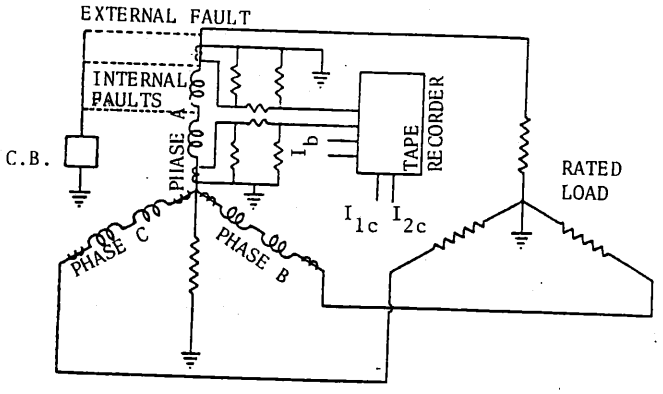


Fig. 5. Test equipment configuration used for fault simulations.

The operation of the digital protection scheme was tested with the following four types of faults applied to the alternator:

1. Internal single phase faults involving 50 percent of the stator winding.
2. Internal single phase faults involving 100 percent of the stator winding.
3. Internal two phase faults involving 50 percent of the stator winding.
4. External single phase faults.

Fourty-five type 1 internal faults were simulated. In twenty of these, the inception of the fault was controlled by using a synchronous switch in place of the circuit breaker of Fig. 5. Four groups of five faults each, were applied with fault incidence delayed approximately 0^o, 30^o, 60^o and 90^o from the zero crossing of the terminal voltage waveform. The remaining twenty-five type 1 simulations were recorded without incidence control. Twenty-five each of types 2, 3 and 4 faults were also simulated in this manner. In the two phase fault simulations, the 50 percent points of the stator windings were shorted through a current limiting resistor. The fault monitor threshold was set at 50 millivolts. The analog computer gains were adjusted so that one per unit generator current was represented by a

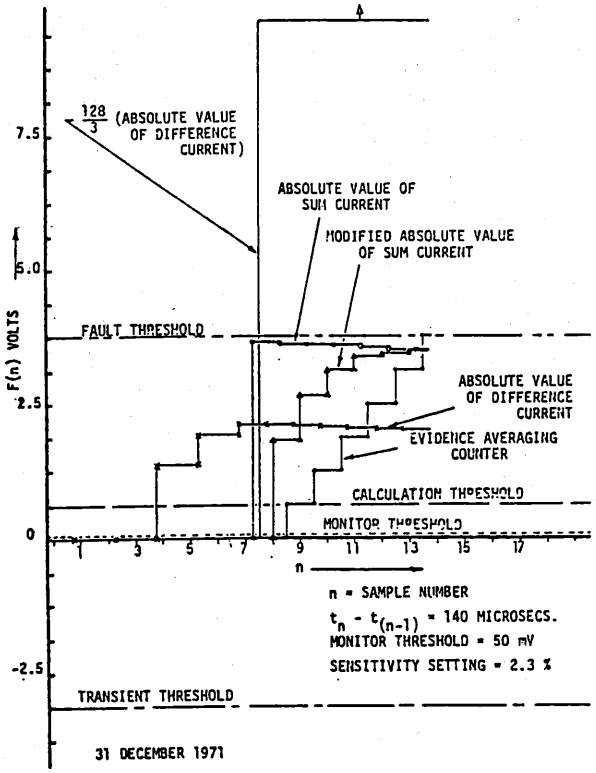


Fig. 6. Reaction of the protection system to a type 1 fault without incidence control.

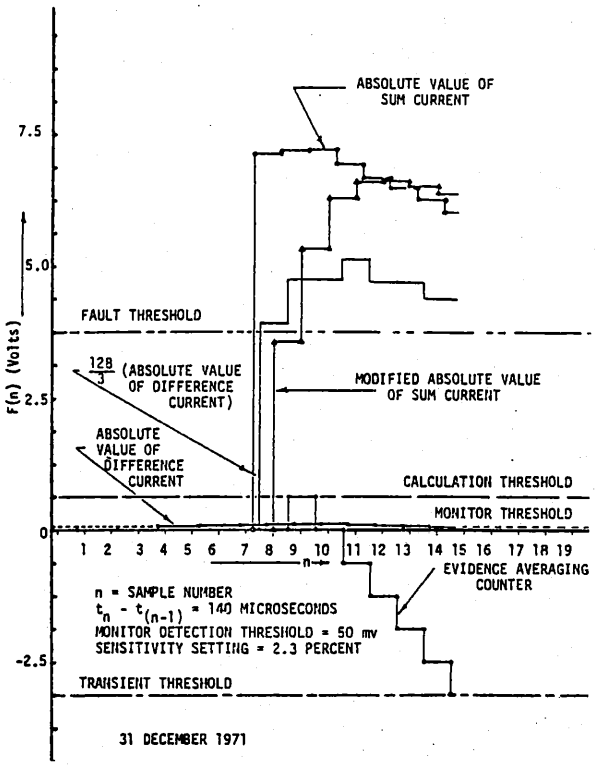


Fig. 7. Reaction of the protection system to a type 4 fault.

sinusoid of 2.5 volts peak value in the digital computer. Out of all the studies reported by the authors, two cases are reproduced here.

Type 1 faults

The data from each fault was recorded and was examined by the protection scheme several times. All the type 1 fault simulations were examined with the relay sensitivity set at 2.3, 3.1 and 3.9 percent. The reaction of the scheme to one of the type 1 faults, as reported by the authors, is presented in Figure 6. All functions are plotted in the time sequence in which they were sampled or generated. The reconstructed difference current function indicates that the fault probably occurred just after the second sample shown, and exceeded the monitor threshold in sampling interval 3. With such a large difference current, this sample was the largest of the three compared in the first pass for phase allocation. The second post-fault sample of the difference current of this phase was again found to be the largest. The phase allocation segment then transferred control to the proper verification routine. The next sample of difference current was taken as part of fault verification. During the first pass through this routine, the modified absolute value of the sum current was generated as zero because no sum current samples had been read prior to the first calculation. The difference current was multiplied by 128. No comparison between the modified sum current and the difference current was made since the former had not yet exceeded the calculation threshold. On the second and subsequent passes for verification, the modified sum current exceeded the calculation threshold. Three times the modified sum current and 128 times the absolute value of the difference current were compared. This lead to the conclusion that the generator was experiencing a fault. The varification process was repeated and every time a fault decision was indicated, the evidence averaging counter was incremented. The program was interrupted and printing initiated when the counter "COUNT" reached the fault threshold. In a power system application a trip command would be issued at this stage.

The authors have reported that, in all cases mentioned above, the phase allocation sequence of the protection scheme correctly selected the faulted phase for verification. The decision making in each of these cases was correctly concluded in less than three milliseconds. The various sensitivity settings did not affect the operating times of the relay.

Type 4 faults

External faults were simulated and examined to test the ability of the protection scheme to descriminate between in-zone and out of zone faults. As indicated earlier, one generator terminal was short circuited to ground. The operation of the protective scheme, using the sensitivity settings of 2.3, 3.1 and 3.9 percent, was tested. The reconstruction of a typical case is presented in Figure 7. As indicated by the reconstructed response, imperfect current gains introduced some errors. All cases were, however, correctly verified as transients not warranting trip initiation. The relay sensitivity was increased to 1.6 percent to test its susceptibility to noise. The fault studies were repeated; in nine of the 25 cases, the conclusions made by the relay were erroneous (stator is faulted). This setting is much lower than 5 - 25% usually adopted and was tried only to test the relay's susceptibility to noise. The authors have reported that, in all cases, the relay selected the faulted phase correctly for fault verification.

CROSSCORRELATION FUNCTIONS APPROACH

It is shown in reference [67] that the real and imaginary components of a current phasor, I, can be

determined by a digital computer using the following two correlation functions.

$$I_d = \frac{1}{N} \sum_{k=1}^{N} i\,(k\Delta T)\,\sin\,(\omega k\Delta T) \qquad \ldots(1)$$

$$I_q = \frac{1}{N} \sum_{k=1}^{N} i\,(k\Delta T)\,\cos\,(\omega k\Delta T) \qquad \ldots(2)$$

where: $T = 2\,\frac{T}{N}$

N is the number of samples of a current taken in one cycle and

T is the time duration of ½ cycle at fundamental frequency.

Hope, Malik and Dash [67] used Equations 1 and 2 to determine the d and q components of the line and neutral side currents (I_1 and I_2) of each phase of the generator being protected. The line and neutral side currents were then expressed in the phasor form as follows:

$$I_1 = I_{d1} + j\,I_{q1} \qquad \ldots(3)$$

$$I_2 = I_{d2} + j\,I_{q2} \qquad \ldots(4)$$

The following two operating and two restraining signals were derived for use in the differential relays.

$$S_{o1} = |I_1 - I_2| = [(I_{d1}-I_{d2})^2+(I_{q1}-I_{q2})^2]^{\frac{1}{2}} \qquad \ldots(5)$$

$$S_{r1} = |I_1 + I_2| = [(I_{d1}+I_{d2})^2+(I_{q1}+I_{q2})^2]^{\frac{1}{2}} \qquad \ldots(6)$$

$$S_{o2} = (I_{d1}-I_{d2})^2+(I_{q1}-I_{q2})^2 \qquad \ldots(7)$$

$$S_{r2} = I_{d1}I_{d2} + I_{q1}I_{q2} \qquad \ldots(8)$$

Two versions of the digital differential relay were developed using these signals. The first version used the currents calculated by Equations 5 and 6 as operating and restraining functions. The relay produced a trip signal when S_{o1} exceeded $F_s S_{r1}$; F_s being a prespecified sensitivity factor. The second version used the signals generated by Equations 7 and 8 for operating and restraining purposes. The proposed algorithms were implemented on an HP 2100 minicomputer. Six sample and hold circuits and 10 bit A/D converters were used to sample data at 960 Hz. The line and neutral currents were converted to the form of voltages using shunts and amplifiers. Six pole, 6450 Hz Butterworth low pass filters were used for preprocessing the input signals before conversion to the digital form.

Testing the Relays

The authors tested the relays in a laboratory set up similar to that used by Sachdev and Wind [36] except that, in some of the tests, the generator was connected to an infinite bus through a transmission line. The generator used in this case was a 5 kVA 208 Volts three phase machine. A grounding resistance was used to limit the single phase to ground fault currents to 2 p.u. The performance of the relays was tested by applying the following faults to the generator.

1. Internal single phase faults involving 50 percent of the stator winding.
2. Internal phase-phase faults involving 50 percent of the stator winding.
3. Internal single phase and two phase faults involving 100 percent of the stator winding.
4. External single phase, two phase and two phase to ground faults.
5. Internal single phase and two phase faults involving 50 percent of the stator winding with the generator connected to the infinite bus through a resistor and an inductor simulating a short transmission line.

The faults were applied to the generator from the computer by sending a signal, via a D/A converter, which triggered a set of SCR's. In some cases, the incidence of the fault was controlled such that the fault was applied at approximately 0°, 30° and 90° after the zero crossings of the terminal voltage.

One of the internal single phase to ground fault studies reported in Reference 67 is reproduced in Figure 8. In this case, two single phase to ground faults were applied on 50 percent of the generator winding when the generator was supplying an isolated load. The fault incidences were controlled to be at 0 and 90 electrical degrees after the zero crossings of the voltage waveforms. The operating signals, S_{o1}'s, and the restraining signals, $F_s S_{r1}$'s, for sensitivity factors of 0.06, 0.09 and 0.15 are shown in the Figure. A study of this figure shows that when the fault incidence is 0° and a sensitivity factor of 0.15 is used, the operating signal exceeds the restraining signal 6 msecs. after the inception of the fault. The operating signal exceeds the restraining signal in 4 msecs when the sensitivity factor is reduced to 0.06.

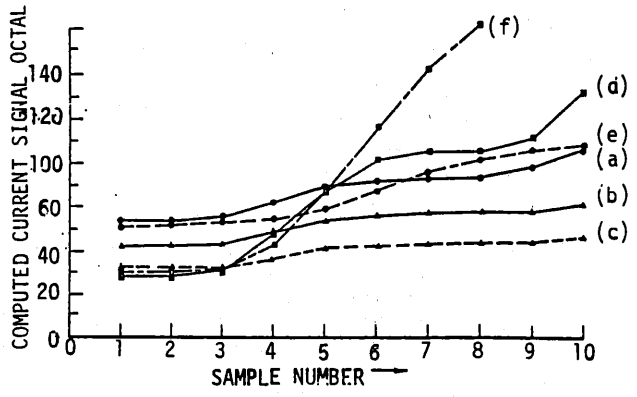


Fig. 8. Internal phase-to-ground fault. 1 p.u. current equals Octal 200.

Restraining Signals:	(a)	F_s=0.15;	FI=0°
	(b)	0.09;	0°
	(c)	0.06;	0°
	(e)	0.15;	90°
Operating Signals:	(d)		0°
	(e)		90°

Figure 9 depicts the operating and restraining signals (S_{o2} and S_{r2}) generated by using Equations 7 and 8 for a line to ground and a line to line fault at the mid points of the windings, and an external fault. It is obvious from this figure that the use of S_{o2} and S_{r2}

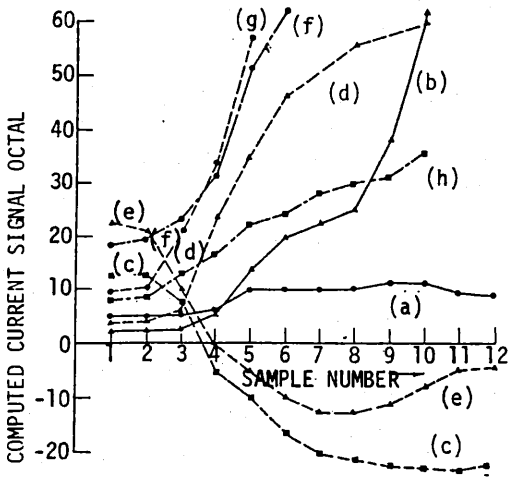


Fig. 9. Protection scheme characteristics for restraining function of Equation 8.
Restraining Signals: (a) L-G Fault (50%) (c) L-G Fault (50%) with system connected (e) L-L Fault (50%) with system connected (g) external fault (L-G)
Operating Signals: (b) L-G Fault (50%) (d) L-G - with system connected (f) L-L Fault (50%) with system connected (h) external fault

seem to slightly increase the operating speed of the relay. The authors also demonstrated that the use of S_{o2} and S_{r2} increased the relay's insensitivity to external faults.

SECOND HARMONIC CURRENT APPROACH

Hope, Dash and Malik [75] proposed a novel approach for detecting unsymmetrical generator faults. The approach takes advantage of the phenomenon that a second harmonic component is present in the field current during unsymmetrical system faults. The negative sequence power is monitored at the terminals of the machine and the direction of its flow is used to determine whether the fault is internal or external to the generator. During internal faults the negative sequence power flows from the generator to the system, whereas, it flows from the system to the generator during external faults. As in the differential relay, the authors used the correlation technique in the development of this relay. Equations 1 and 2 are used to estimate the second harmonic component in the field current. Phase voltages and currents observed at the terminals of the alternator are processed in a similar manner to determine their real and imaginary components. The real and imaginary components of the negative sequence voltage and current are then determined using the following equations.

$$I_{f2} = [I_{df2}^2 + I_{qf2}^2]^{\frac{1}{2}} \quad \ldots(9)$$

$$V_\phi = V_{d\phi} + j\, V_{q\phi} \quad \ldots(10)$$

$$I_\phi = I_{d\phi} + j\, I_{q\phi} \quad \ldots(11)$$

$$V_n = V_{dn} + j\, V_{qn} \quad \ldots(12)$$

$$I_n = I_{dn} + j\, I_{qn} \quad \ldots(13)$$

where: I_{f2} is the second harmonic component of the field current.
V_ϕ is the phase voltage; ϕ = a,b,c.
I_ϕ is the phase current.
V_n is the negative sequence voltage.
I_n is the negative sequence current.

The real and imaginary components of the negative sequence voltage were calculated by Equations 14 and 15 from the phase voltage components, $V_{d\phi}$ and $V_{q\phi}$. Similar equations were used to calculate the real and imaginary components of the negative sequence current.

$$V_{dn} = \frac{1}{3}\left[V_{da} - \frac{1}{2}(V_{db}+V_{dc}) + \frac{\sqrt{3}}{2}(V_{qb}-V_{qc})\right] \quad \ldots(14)$$

$$V_{qn} = \frac{1}{3}\left[V_{qa} - \frac{1}{2}(V_{qb}+V_{qc}) - \frac{\sqrt{3}}{2}(V_{db}-V_{dc})\right] \quad \ldots(15)$$

The operating characteristic of the relay, proposed by Hope et. al. [75], is shown in Figure 10. The operating and restraining signals are the second harmonic component of the field current and the negative sequence power at the generator terminals respectively. To reduce the possibility of spurious tripping, it was made conditional that both signals attain a minimum threshold before a trip signal is generated.

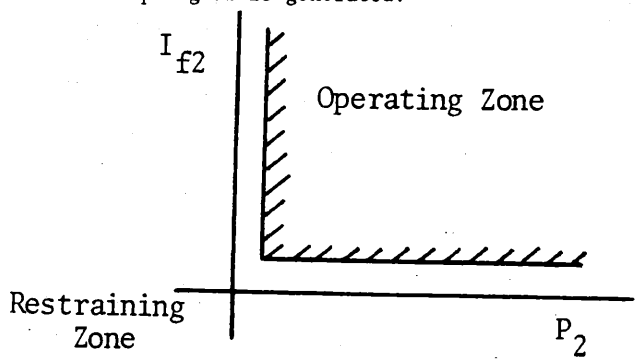


Fig. 10. Operating characteristics of the negative sequence power relay.

This relay was also implemented on an HP 2100 minicomputer and the data was sampled at 960 Hz. Low pass filters were used to limit the frequency of the input signals provided to the sampler.

Testing the Relay

The equipment used in this set up was the same as used in the differential relay of Reference 67. The experimental set up used in this case is shown in Figure 11. In this work, the operation of the relay was tested for the following faults.

1. Internal phase to ground and phase to phase faults on the midpoint of armature winding.
2. Internal phase to ground faults on the generator terminals involving 100% of the armature winding.
3. Inter-turn faults.
4. External phase to ground, phase to phase and two phase to ground faults on the generator terminals.

The operation of the relay for a single phase to ground fault at the midpoint of a generator phase is shown on the I_{f2}, P_n plane in Figure 12. The trajectory enters the operating zone in about 6 msecs. The P_n versus I_{f2} trajectory for a phase to phase external fault

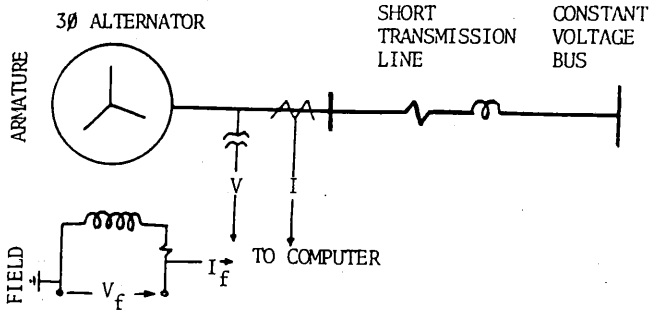


Fig. 11. Single line diagram of the experimental set up.

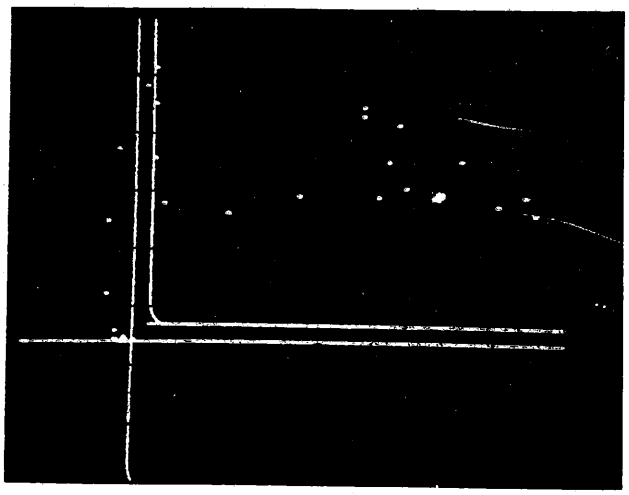


Fig. 12. P_n-I_{f2} trajectory for a single phase to ground fault at the midpoint of phase 'b'.

is shown in Figure 13. The result shows that, for such faults, the operational vector stays well within the restraint zone.

DIGITAL COMPUTER PROTECTION OF HYDRO POWER PLANTS

Some features of digital computer protection of hydro plants have been discussed by Sachdev [Some Aspects of Digital Computer Protection of Hydro Power Plants, IEEE Pub. 76CH1057-9REG5, pp. 82-86.]. Factors dictating the selection of frequency for sampling data have been discussed from a systems point of view. The philosophy of using protection and data acquisition computers in an interactive mode is then discussed. The suitability of using multi-microprocessor approach for the protection of a turbine-generator has also been examined.

Sampling Frequency

Protecting functions performed in a hydro power plant are numerous. Some of these functions are to reveal the presence of mechanical abnormalities whereas the others are to detect electrical faults. Most electrical faults can be classified into one of the following types:

1. Generator differential unbalance.
2. Generator-Transformer differential unbalance.
3. Generator stator ground.

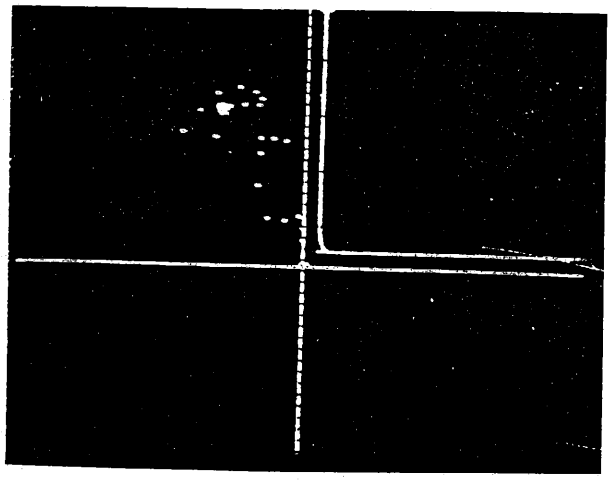


Fig. 13. P_n-I_{f2} trajectory for a two phase external fault.

4. Generator current unbalance.
5. Overcurrent (with voltage restraint).
6. Overvoltage.
7. Overfrequency/underfrequency.
8. Field failure.
9. Field ground.

Relays provided for the protection of generators and transformers are excited from current and voltage transducers. It can be shown that a minimum of twenty one signals have to be monitored for detecting the faults listed above. This number is arrived at by assuming that each set of current and voltage transducers provide the three phase quantities and a zero sequence quantity. It is also assumed that one signal each of field current, generator speed and A/D caliberation check are used in detecting abnormal conditions. It is preferable to sample the currents and voltages simultaneously and, therefore, A/D converters with sample and hold facility may have to be used. Once a set of samples have been obtained and placed on hold, a digital computer can receive them one at a time. Assume that the computer used for plant protection can receive one sample every 20 μsecs and one half of the intersampling time can be used for computing. In this manner, the total computing time before another set of data is due to be received, depends on the rate at which system data is sampled. The process of the computer receiving samples and the intersampling time which can be used for computing are graphically shown in Figure 14. The total computing time per sampling cycle is given as a function of the frequency of receiving system data in Table 1. It is obvious that the total computing time per sample cycle decreases as the

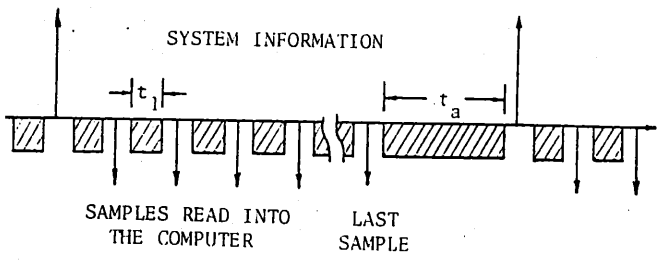


Fig. 14. Distribution of data sampling and computing time.

Table 1. Computing time per sampling interval available for different sampling rates adopted for digital computer protection of a hydro plant.

A	B	C	D
400	210	2080	2290
800	210	830	1040
1000	210	580	790
1500	210	265	475
1600	210	205	415
2000	210	80	290
2380	210		210

A: Sampling Frequency (Hz)
B: Computing Time (Σt_1) μ Secs
C: Computing Time (ta) μ Secs
D: Total Intersampling Computing Time μ Secs

sampling frequency increases. The sampling frequency for a computer protection scheme should therefore be selected such that:

(i) the computed information is reasonably accurate.

(ii) dectection and verification of faults is completed after receiving a set of data and before the next set of samples start arriving.

The first of the above two conditions is essential whereas the second is only a desirable feature.

In addition to the twenty one samples required for detecting electrical faults, a digital computer may have to supervise functions such as, coolant flows; oil and compressed air pressures; generator winding, field winding, bearings, oil and coolant temperatures etc. Some of these abnormalities will require that the unit be tripped while the others require that an operator be alerted either at the plant or at a central control location.

Integrated Operation

Considering that the temperature, pressure, level, flow and electrical signals for detecting abnormalities may number over one hundred per generating unit, a large part of a protection computer's time will be used in receiving input data from the sample and hold devices. To save this time, a multi-processor system may be used. One such system is shown in Figure 15. A special purpose c.p.u. can be exclusively used to communicate with the system, i.e. receive information from the sampling devices and place it in a block of common memory, and pass on instructions to the digital to analog convertors for issuing alarms and tripping the machine. One c.p.u. and its associated equipment i.e. c.p.u. P-1, memory unit 1, an input-output device and a disk unit, can be used to perform the protective functions. Another c.p.u. which may be part of a data acquisition computer, can share the common memroy block in which the special purpose c.p.u. continuously places data. This part of the integrated computer system can also act as a standby for protection functions. It can also be used to receive processed fault data from the protection computer and print it for operator's scrutiny. This feature will ensure that the protection computer is exclusively used for the function it is provided for.

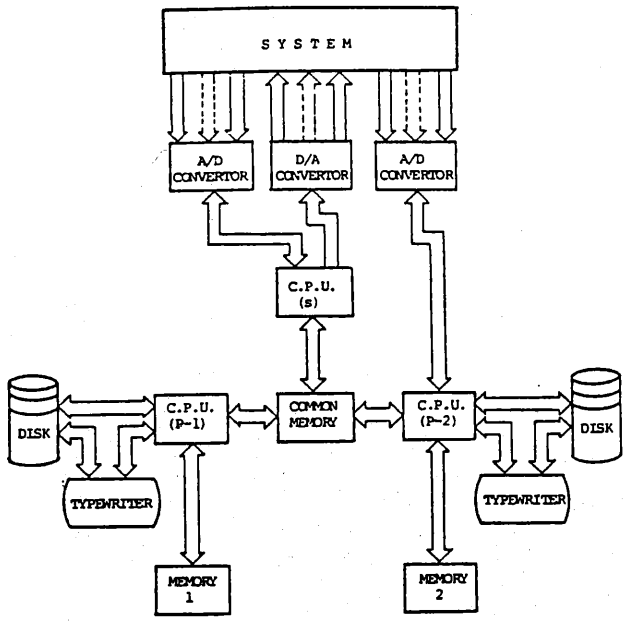


Fig. 15. A multi-processor system for protection and data acquisition.

Multi Microprocessor Approach

In the arrangement suggested above, a minicomputer is used to protect one hydro unit. This is like putting all eggs in one basket. An alternate approach consists of dividing the protection functions, listed earlier in this paper, between a few microprocessors, say four in this application. It will be desirable, not to allocate more than one critical function to any one processor. Keeping this consideration in mind, the protection functions may be assigned to four microprocessors as follows:

Microprocessor 1: Generator differential unbalance and current unbalance.

2: Overcurrent with voltage restraint and field failure.

3: Generator-transformer differential unbalance.

4: Overvoltage, overfrequency, field ground and stator ground fault.

Assume that the protection functions are allocated as above, sampling rate is 1 kHz and a microprocessor takes 20 μsecs to receive a sample from the A/D converter. Current, voltage and calibration check samples received, c.p.u. time used in receiving samples and the cpu time available for computing during each intersampling interval, would be as in Table II.

A perusal of this table indicates that each microprocessor will have over 800 μsecs per sampling interval for processing data and making decisions. This time is slightly more than 790 μsecs available in the single minicomputer protection scheme discussed earlier. Microprocessors are in general slower than minicomputers. This disadvantage will be considerably offset by the increase in total computing time per sampling interval and the increased computing speed of the newer generation of microprocessors.

Table II. Computing time per sampling interval available in a multi-microprocessor system.

Function	Microprocessor No.			
	1	2	3	4
No. of current samples	8	4	8	2
No. of voltage samples	-	4	-	3
Calibration check sample	1	1	1	1
Cpu time for obtaining samples - secs.	180	180	180	180
Cpu time available for computing - secs.	820	820	820	880

In the single minicomputer approach a disc and a typewriter was suggested to be used with each minicomputer. If the same approach is used in the multi-microprocessor arrangement, the cost of peripheral devices in the above example will increase four fold. To reduce the equipment cost, a set of peripherial devices may be shared between four or more microprocessors. The peripherial devices can be connected to each microprocessor, on a predetermined priority basis, by a special purpose input-output c.p.u.

The philosophy of system protection adopted so far includes using backup relays which may be installed either at the location of primary relays or at remote locations. Most major utilities are using duplicate relays for critical protective functions. In the initial stages, digital computer protection may be supplemented with a full contingent of electromechanical and solid-state relays. The availability of the microprocessor system for protection of a generating unit can also be improved by incorporating redundant microcessor and automatic changeover relays. A set of standby input-output devices can also be used to further increase the effectiveness of the proposed approach.

SUMMARY

Protection of generators by digital computers has been discussed in this chapter. An arrangement of minicomputers for data acquisition and plant protection has been presented. Multi-microprocessor approach for the protection of a hydro generator from electrical faults has been briefly discussed. Three different approaches for the differential protection of generators have also been presented. It is demonstrated that digital processor approaches can detect generator winding faults and can discriminate these faults from those external to the unit.

CHAPTER VII

TRANSFORMER DIFFERENTIAL PROTECTION

Algorithms for digital relays have been presented in Chapter III. Three digital processor systems which provide distance protection of transmission lines have been described in Chapter IV. In Chapter V, unconventional approaches to transmission line protection have been presented. Methods of protecting generators using digital computers have been outlined in the last chapter. Three approaches to transformer differential protection are presented in this chapter.

G.D. Rockefeller [7] suggested a procedure of providing transformer differential protection as an integral part of an overall approach to substation protection with a digital computer. Sykes and Morrison [26] used recursive digital filters in the design of a harmonic restraint transformer differential relay. Data from simulated faults and current inrush phenomenon were used to test the proposed approach. Malik, Dash and Hope [60] used correlation technique for determining the components of fundamental and second harmonic frequencies in the 'operate' and 'restraint' currents. These authors also tested their approach using simulated data. Schweitzer, Larson and Flechsig [71] used finite impulse response (FIR) filters for differentiating between transformer faults and magnetizing inrush. The proposed algorithm was implemented by Larson et. al. [87] on a Motorola MC6800 micro-processor for use as a transformer differential relay. This device was tested in a laboratory using a 500 VA transformer. Each approach uses the current differential technique and a software program in a digital computing device.

This chapter briefly presents the essential features of the transformer differential protection schemes listed above. Some of the results obtained by applying these approaches are also included. Before presenting the digital protection schemes, the principle of transformer differential protection is briefly outlined.

DIFFERENTIAL PROTECTION OF A DELTA-WYE TRANSFORMER

Figure 1 depicts a typical differential protection arrangement for a delta-wye transformer and harmonic restraint supervisions [59]. Currents in the primary and secondary windings are not equal because:

(i) the transformation ratio is usually not 1.0,
(ii) the primary currents include magnitizing and core loss components and
(iii) phase displacements between the primary and secondary currents due to delta-wye transformation.

The differences in phase angles of the primary and secondary currents are usually taken care of by connecting the delta side C.T.'s in wye and wye side C.T.'s in delta. The current transformer ratios are selected such that during normal loads currents in the relay leads connected to the primary and secondary C.T.'s are in phase and are equal in magnitude.

In the work on differential protection by digital computers proposed in the past [26,60,71,87] and discussed in this chapter, a single phase transformer and its model were used for testing the relays. The focal point of the work has been to distinguish magnetizing in-rush currents from currents due to internal faults.

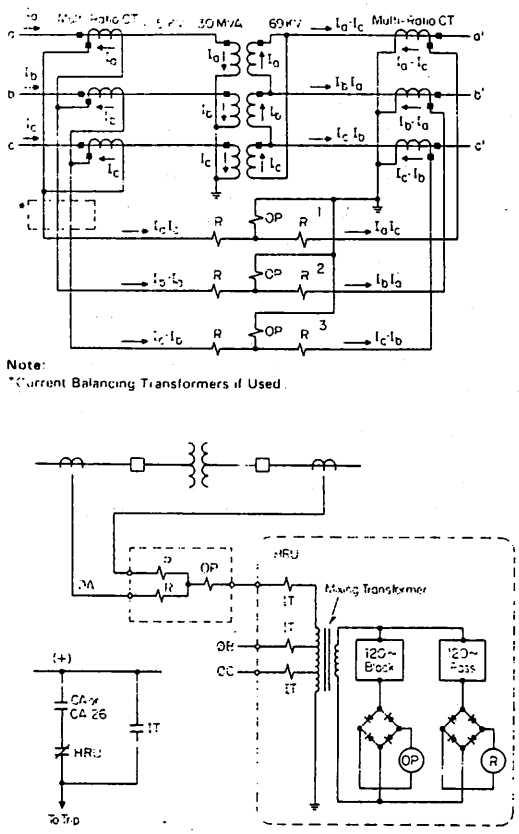


Fig. 1. (a) Phasing check for a transformer differential relay.
(b) Arrangement for including harmonic restraint relay in a transformer differential protection arrangement.

WAVE SHAPE IDENTIFICATION APPROACH

Rockefeller [7] suggested that the magnetizing inrush current can be identified by monitoring the time durations between successive peaks of the differential current. In a 60 Hz system successive current peaks are experienced 8 msecs apart (½ cycle) during external faults. This is true before C.T. saturation sets in. This phenomenon is demonstrated in Figure 2.a; if P and P' are considered to be the two successive peaks, these are approximately 8 msecs apart. Two types of waveforms are experienced due to magnetzing in rush [7]; the successive peaks are either 4 msecs. or 16 msecs. (approximately) apart. It was, therefore, proposed that legitimate fault currents may be recognized by two successive peaks being 7.5 to 10 msecs. apart. Another requirement suggested is that a peak be 75 to 125 percent of the previous peak and of opposite sign. The instants of current peaks were proposed to be detected by monitoring the change of sign of the difference between two successive samples of a current.

In reference [7] , Rockefeller suggested the use of percent differential characteristic as shown in Figure 3. Because a transformer is likely to be

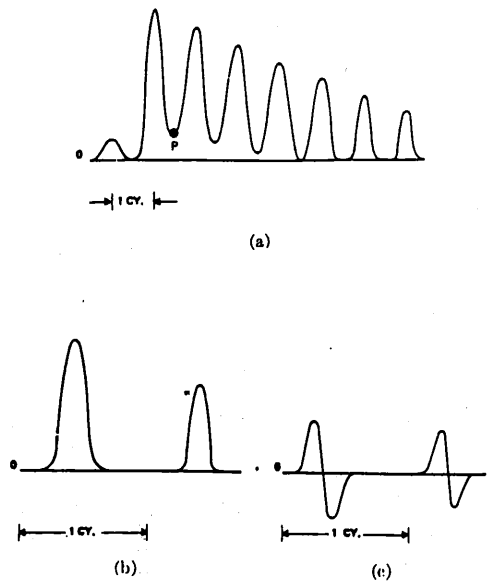


Fig. 2. Some differential current waveforms. (a) Dc saturation of current-transformer during external fault. (b) Inrush. (c) Inrush.

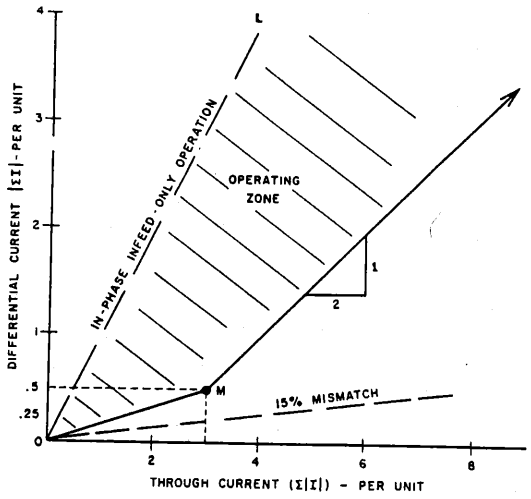


Fig. 3. Percent differential characteristic (PDFC).

operated at off-nominal taps, atleast fifteen percent mismatch was therefore, proposed to be permitted. Due to mismatch of C.T. ratios the differential current increases. It was therefore proposed that the slope of the relay characteristics be increased for through currents in excess of 3.0 p.u.

RECURSIVE BANDPASS FILTER APPROACH

Sykes and Morrison [26] used the harmonic-restraint approach for differential protection of transformers using a digital computer. The block diagram [26] describing the approach is given in Figure 4. A twenty msecs. delay is included in the 'operate' path to prevent false tripping on transient filter outputs associated with magnetizing inrush. The delayed differential signal is applied to a 50 Hz bandpass filter whose output is rectified and then smoothed by a 10 Hz lowpass filter to provide the 'operate' signal. (The relay was developed for a 50 Hz system). Second harmonic component is small at the start of an inrush. The restraint signal was therefore amplified and applied to a 100 Hz bandpass filter to obtain the second harmonic component. This component was also rectified and smoothed to obtain the 'restraint' signal. The operate and restrain signals were then compared to decide if the transformer is experiencing a fault or an in-rush condition.

The 50 and 100 Hz bandpass filters were realized using Equations 1 and 2. The lowpass filter was realized using Equation 3. Frequency responses of these filters [26] are reproduced in Figure 5.

$$y_n = 0.096x_n - 0.096x_{n-1} + 1.810y_{n-1} - 0.905y_{n-2} \quad (1)$$

$$y_n = 0.045x_n - 0.045x_{n-1} + 1.580y_{n-1} - 0.953y_{n-2} \quad (2)$$

$$y_n = 0.0087x_n + 1.904y_{n-1} - 0.913y_{n-2} \quad (3)$$

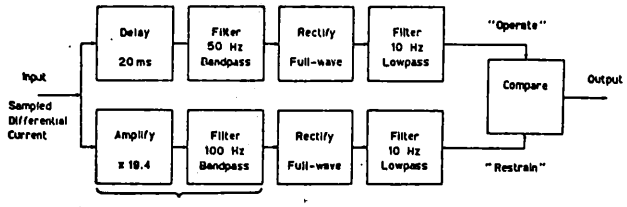


Fig. 4. Block diagram of the transformer differential protection showing the sequence of operations.

Testing the Relay

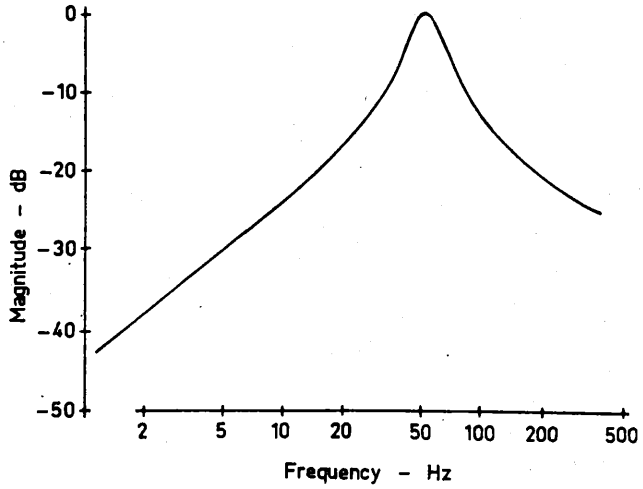
The proposed technique was tested by off-line simulations of faults and magnetizing inrush in single phase transformer. The differential current sampled at 1.0 kHz was processed as described in the last paragraph. Figure 6 depicts the performance of the relay to a simulated in-rush condition with rapidly decaying residual flux. It is obvious that the relay generated adequate restraint signal during this condition. The performance of the relay during a simulated internal fault is shown in Figure 7. The inception of the fault corresponds to maximum D.C. offset. Appreciable restraint signal is present during the internal fault because the 100 Hz bandpass filter does not attenuate the 50 Hz signal adequately.

CROSS-CORRELATION APPROACH

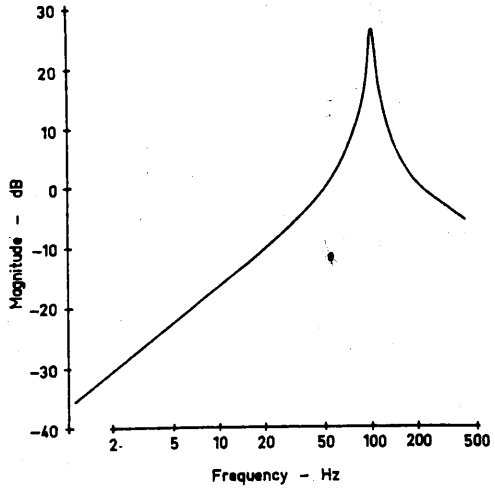
The cross-correlation approach was proposed and used by Malik, Dash and Hope [60]. As reported in Chapters III and VI, the cross-correlation functions between the current waveforms and reference sine and cosine waveforms provide the following correlation functions.

$$\phi_i = \frac{1}{2} I_n \cos \theta_n \quad (4)$$

$$\phi_i' = \frac{1}{2} I_n \sin \theta_n \quad (5)$$



[a]



[b]

Fig. 5. Frequency response of (a) the 50 Hz band-pass filter and (b) the 100 Hz band-pass filter.

The peak values of the nth harmonic can be obtained from these equations using Equation 6. It is important to appreciate that cross-correlation functions are obtained by integrating the weighted input signal over a period of one cycle of the frequency of interest.

$$I_n = 2 \left[(\phi_i)^2 + (\phi_i')^2 \right]^{\frac{1}{2}} \qquad (6.a)$$

$$\theta_n = \tan^{-1} (\phi_i' / \phi_i) \qquad (6.b)$$

In addition to using the cross-correlation functions between the currents and reference sinusoids, Malik et. al. [60] used cross-correlations with even and odd square waves shown in Figure 8. The advantage of using the square waves as weighting functions is that, in this case, the computation of correlation functions consists of additions and subtractions only.

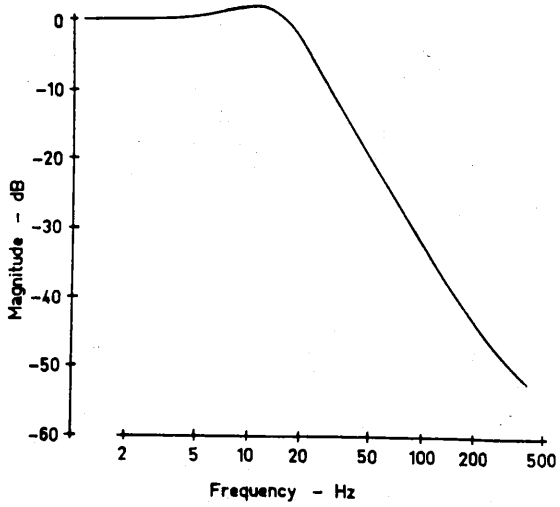


Fig. 5(c). Frequency response of the 10Hz low-pass filter.

The peak value of the current is, however, computed by using Equation 7.

$$I_n = \frac{\pi}{2} \left[(\phi_{iI})^2 + (\phi_{iI}')^2 \right]^{\frac{1}{2}} \qquad (7)$$

Testing the Relay:

The authors used analog filters to preclude from the inputs frequencies higher than the seventh harmonic (420 Hz). Sampling rates of 960 and 480 Hz and one cylce data window were used. The relay was programmed and tested off-line on a CDC 6400 computer. Internal faults and magnetizing inrush currents were formulated numerically assuming that the rates of saturation to magnetizing flux densities (B_s/B_m), residual to magnetizing flux densities (B_r/B_m) and saturated reactance are 2.0, 0.5 and 0.25 (p.u.) respectively. Residual flux decay rates of 577 and 115.4 msecs. were tried. Some of the results reported by the authors [60] are reproduced in this section.

Figure 9 shows the outputs representing the 'operate' and 'restraint' signals obtained by using the sine-cosine cross-correlations during a simulated internal fault. This figure shows that the 'operate' signal exceeds the 'restraint' signal 10-12 millisecs after the inception of the fault. Figure 10 depicts the restraint and operate signals obtained by using the cross-correlation between square waves and the transformer currents obtained from an internal fault. In this case, the 'operate' signal exceeds the 'restraint' signal in approximately twelve msecs. Figures 11 and 12 show the 'restraint' and 'operate' signals produced during a magnetizing inrush condition. Results of Figure 11 were generated by using the sine-cosine cross-correlation approach. For the same input data, square wave cross-correlation approach generated the results given in Figure 12. In each case the 'restraint' signal remain in excess of the 'operate' signal and, therefore, no tripping signal is generated.

FINITE IMPULSE RESPONSE APPROACH

Schweitzer, Larson and Flechsig [71] and Larson, et. al. [87] used the finite impulse response filters to detect magnitizing inrush current for use in a digital transformer differential relay. Reference [71] examined the response of the digital filters using simulations.

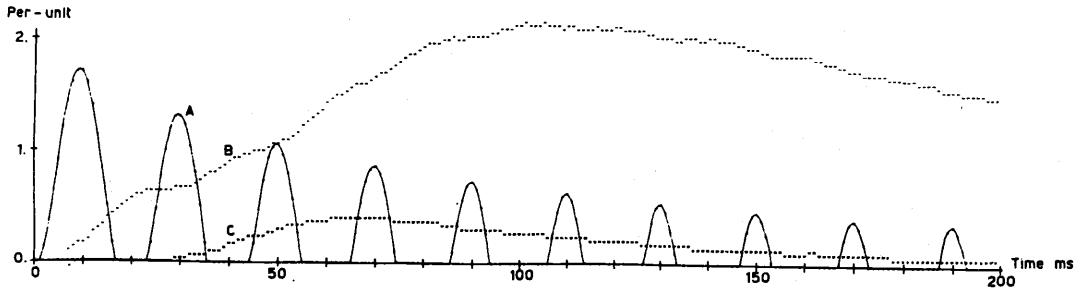


Fig. 6. Performance on simulated inrush with rapid decay.
A - Inrush current.
B - Output of low-pass filter in "restraint" path.
C - Output of low-pass filter in "operate" path.

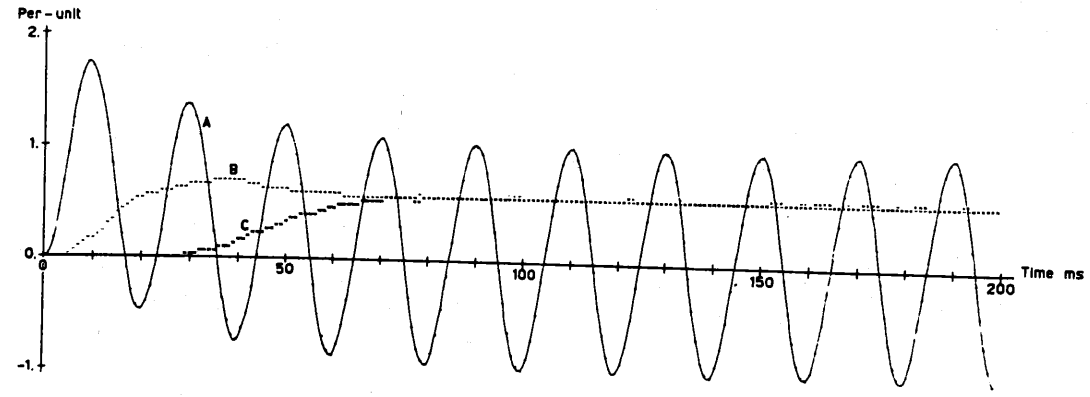


Fig. 7. Performance on simulated internal fault.
A - Fault current.
B & C - as for Fig 6.

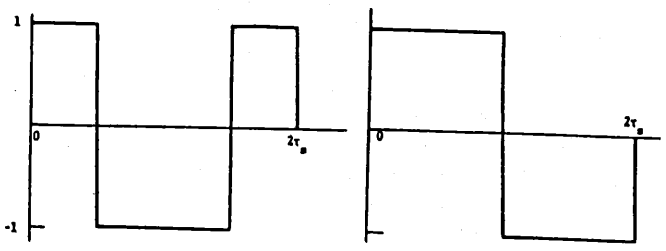


Fig. 8. Time domain orthogonal square waves.

This approach was then used in the design of a transformer differential relay using a Motorola MC6800 microprocessor. The relay was tested in the laboratory environment. This approach is basically similar to the method of odd and even square wave cross-correlation suggested by Malik et. al. [60] except that the criterion for discriminating magnetizing inrush conditions from internal faults is different.

The algorithm basically consists of determining the following four coefficients [87].

$$S_1(k) = \sum_{m=k-1N}^{k-N2} [i_m - i_{m+N12}] \qquad (8.a)$$

$$C_1(k) = \sum_{m=k-1N}^{k-N34} [i_m - (i_{m+N14}+i_{m+N12}) + i_{m+N34}] \qquad (8.b)$$

$$S_2(k) = \sum_{m=k-1N}^{k-N34} [i_m - i_{m+N14} + i_{m+N12} - i_{m+N34}] \qquad (8.c)$$

$$C_2(k) = \sum_{m=k-1N}^{k-N78} [i_m - (i_{m+N18} + i_{m+N14}) + i_{m+N38} + i_{m+N12} - (i_{m+N58} + i_{m+N34}) + i_{m+N78}] \qquad (8.d)$$

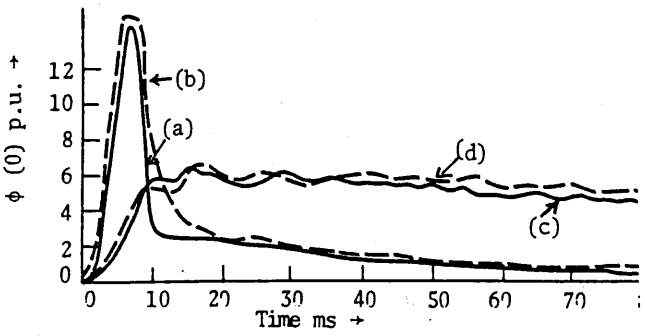


Fig. 9. Sine-cosine function performance with simulated internal fault.
(a) Restraint path crosscorrelation output (N = 16)
(b) Restraint path crosscorrelation output (N = 8)
(c) Operation path crosscorrelation output (N = 16)
(d) Operation path crosscorrelation output (N = 8)

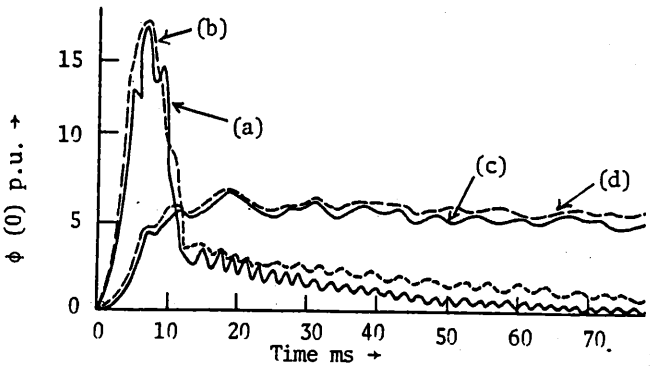


Fig. 10. Odd and even square wave performance with simulated internal fault.
(a) Restraint path crosscorrelation output (N = 16)
(b) Restraint path crosscorrelation output (N = 8)
(c) Operation path crosscorrelation output (N = 16)
(d) Operation path crosscorrelation output (N = 8)

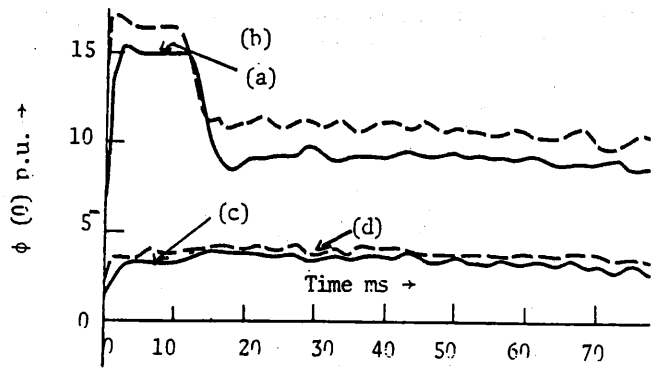


Fig. 11. Odd and even square wave performance with simulated inrush and slow decay.
(a) Restraint path crosscorrelation output (N = 16)
(b) Restraint path crosscorrelation output (N = 8)
(c) Operation path crosscorrelation output (N = 16)
(d) Operation path crosscorrelation output (N = 8)

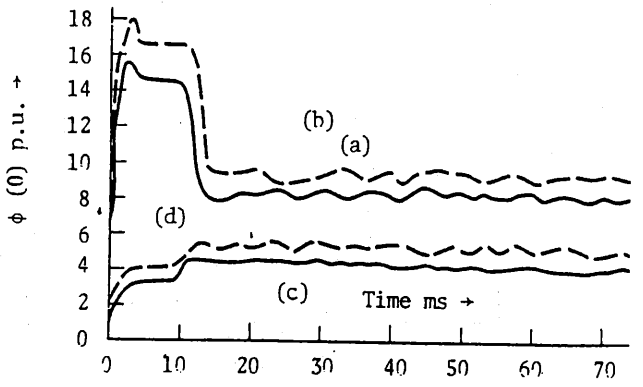


Fig. 12. Crosscorrelation output with simulated inrush and slow decay (N = 16)
(a) Restraint path with sine-cosine functions
(b) Restraint path with odd and even square wave functions
(c) Operation path with sine-cosine functions
(d) Operation path with odd and even square wave functions

where: 1N = N+1; N is the sampling rate per cycle of fundamental frequency

$$N78 = \frac{7}{8}N;\ N34 = \frac{3}{4}N;\ N58 = \frac{5}{8}N;\ N12 = \frac{1}{2}N;$$

$$N38 = \frac{3}{8}N;\ N14 = \frac{1}{4}N \text{ and } N18 = \frac{1}{8}N$$

The frequency responses of these filters for N=∞ are depicted in Figure 13. A study of this figure reveals that:

(i) the outputs of filters S_1 and C_1 are zero for D.C. and even harmonics, and the output is maximum for the fundamental frequency.
(ii) the outputs of filters S_2 and C_2 are zero for D.C. and odd harmonics, and the output is maximum for the second harmonic.

Identification of Inrush Phenomenon

The criterion of discriminating magnetizing inrush from internal faults used by Schweitzer et. al. [71,87] is quite different from the comparison of the fundamental frequency and second harmonic currents used by Malik et. al. [60] and is briefly explained in this section.

The outputs of the four filters obtained by processing the latest samples are examined. The larger of the two components of each pair of filters are determined which are defined as follows.

$$\max(|S_1|, |C_1|) \quad \text{and} \quad \max(|S_2|, |C_2|) \tag{9}$$

It is shown in Reference [71] that the theoretical ratio ξ, $[\max(|S_2|, |C_2|) / \max(|S_1|, |C_1|)]$, lies between 0 and 0.146 during internal faults when the system reactance to resistance ratio is 5 and between 0.334 and 0.586 during magnetizing inrush. This ratio is less than 0.093 during internal faults when the system X/R ratio is 10 or larger. Considering that the system X/R is rarely less than 10, the authors decided to use ξ=0.125 as the threshold value. If ξ is computed to be more than 0.125, it is concluded that a magnetizing inrush condition exists.

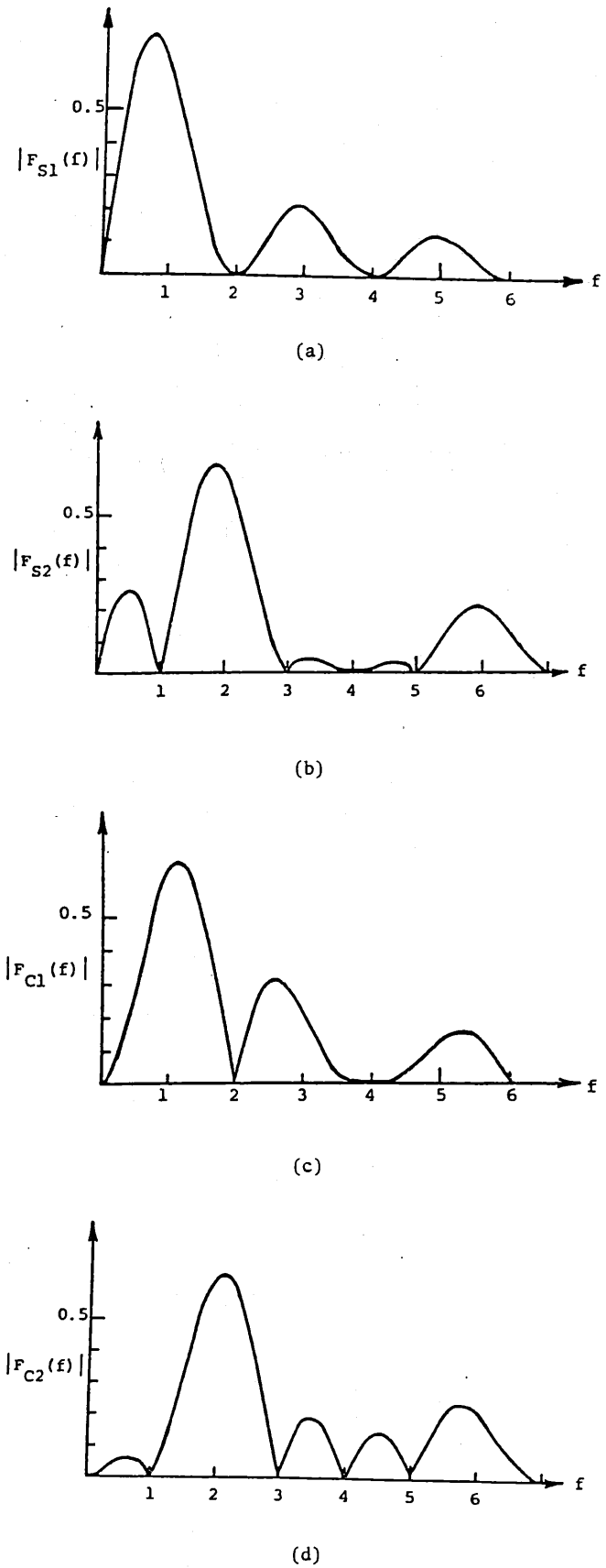


Fig. 13. Frequency response of (a) S_1 filter, (b) S_2 filter, (c) C_1 filter and (d) C_2 filter (f = 1 is normalized system frequency.)

Testing of Algorithm

The proposed algorithm was tested using simulated fault data representing magnetizing inrush and internal fault conditions [71]. Data was considered to have been sampled at 480 Hz. It was observed from these tests that, during some internal faults, the computed values of ξ exceed the threshold temporarily (during the first cycle after the inception of a fault) before settling below the threshold value.

Twenty two cases of magnetizing inrush current were also simulated. Saturation was assumed to occur at 1.4 times the maximum normal operating flux, ϕ_{max}. Two levels of remanent flux (ϕ_R), 0.5 and 0.9 times ϕ_{max}, were considered. Out of twenty two cases, eleven cases actually produced magnetizing inrush. The ratio ξ was found to be more than 0.27 and 0.49 for ϕ_R equal to 0.9x ϕ_{max} and 0.4xϕ_{max} respectively.

Description of the Relay

The algorithm described above was implemented on a Motorola MC6800 microprocessor [87]. The relay characteristic used in this development is shown in Figure 14. Tripings were inhibited if the differential current is less than 0.25 p.u. Relay characteristic was divided into two parts; a slope of 0.25 was used for restraining currents less than 2.5 p.u. and a slope of 0.50 for larger restraining currents. The software flow chart which implemented the relay characteristic is given in Figure 15.

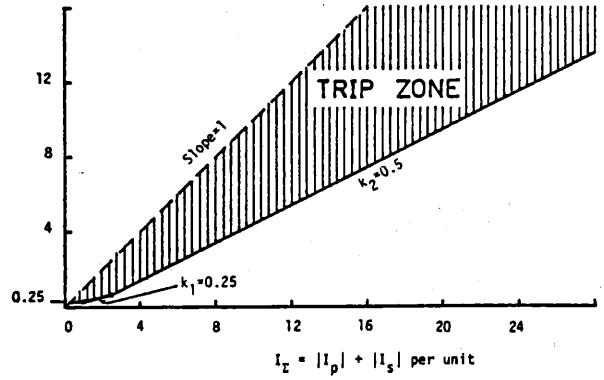


Fig. 14. Differential characteristic used in transformer algorithm tests.

A Sampling rate of 480 Hz was used. Less than one third of the inter-sampling interval is used for the single phase version of the relay equipped with 1MHz clock. Four pole Chebychev low-pass filters were used for signal preprocessing. These filters have 3 dB attenuation at 167 Hz and 20.9 dB at 240 Hz. Sample and hold, multiplexer and 12 bit analog to digital converters were used. A single 8k/16k byte AROM/ROM (read only memory) module was used for storing program which was used for debugging programs stored in RAM (random access memory). Two 2k static RAM modules, one ACIA (asynchronous communication interface adapter) and one input/output module were included. The ACIA provides interface between a teletype and the processor.

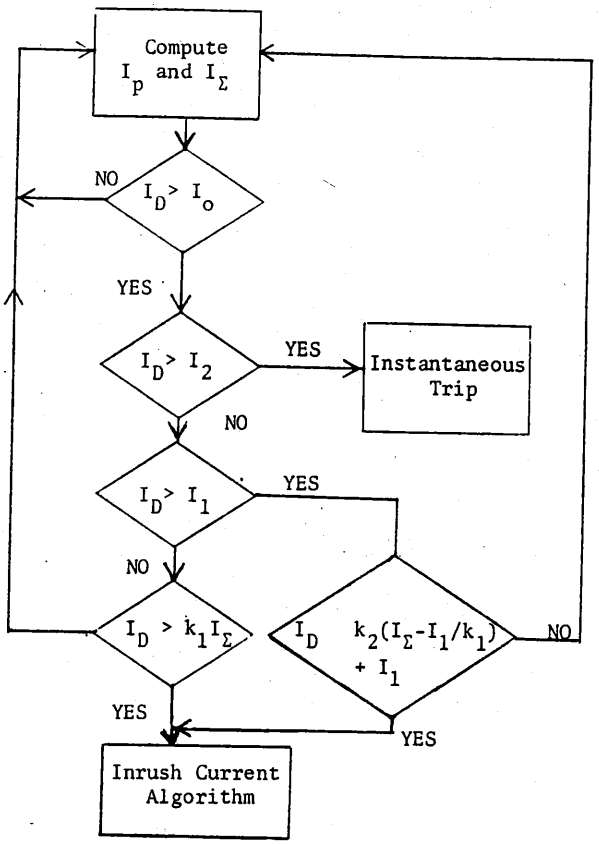


Fig. 15 Flowchart for differential overcurrent algorithm.

Implementation and Testing of the Relay

Figure 16 shows the model system used for testing the transformer differential relay. Four categories of tests were conducted to check the performance of the relay. These categories consists of proving the relay performance during:

(i) inrush current only,
(ii) internal fault only,
(iii) simultaneous inrush and internal fault and
(iv) external fault only.

Sixteen controlled switching operations were tried. All inrush conditions were correctly identified; the computed value of ξ was more than 0.25 whenever an external fault was examined. For limiting the fault current, an autotransformer was used to reduce the input to 28.5 Volts. Internal faults were also applied at controlled switching instants.

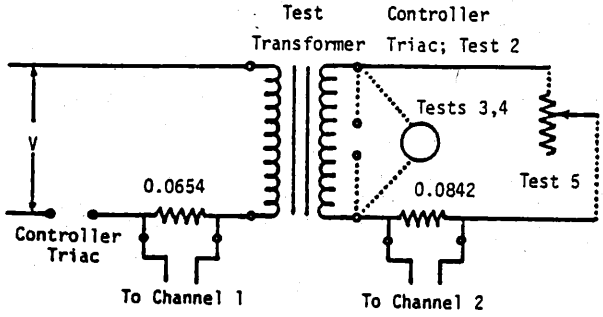


Fig. 16. Model system for inrush and fault current data.

The minimum and maximum relay operating times observed during these tests were 12.6 and 19.1 milliseconds respectively. Relay operating time increased when an internal fault was accompanied with current inrush. In case of a high resistance fault, the largest operating time was 99 msecs. The relay did not operate during external faults. Each pass of the differential relay was tested to take 570 μsecs which is less than one third of the 2.08 msecs intersampling time.

SUMMARY

Differential protection of transformers has been discussed in this chapter. Three approaches tried in the past have been briefly presented. It seems that this area has not received as much attention as the line protection. The work todate, however, indicates that it is possible to design transformer differential relays for implementation on microprocessor based systems.

CHAPTER VIII

RELAY SYSTEMS AND HARDWARE CONSIDERATIONS

This chapter will begin with a general discussion of relaying systems and the limitations of the relaying process. Many of the operating characteristics of a relay are specified in terms of steady-state parameters. A harmonic restraint relay, for example, bases its operation upon the presence of certain harmonics in an input signal. It is assumed at the time of the harmonic estimation that the input signal is in a steady-state. As another example, a distance relay characteristic is described in terms of the impedance of the faulted circuit. Again, impedance is a steady-state concept, and it is calculated under the assumption that a pair of input signals (a voltage and a current) are in steady-state when the relaying decision is made. Since critical relaying decisions are made very soon after the occurrence of a fault, the input signals contain a significant proportion of transient components; the use of steady-state concepts under these conditions requires care and a certain amount of explanation. It is for this reason that the task of extraction of steady-state information from a noisy input signal (i.e. filtering) occupies such a dominant role in most relaying algorithms.

Filtering, whether done with analog circuits, with digital computer algorithms, or with a combination of the two is the usual way of producing specific signal components needed for relaying. A reasonable subject of inquiry is the following: 'What is the best filter for a given relaying application?' More precisely, what is the consequence of using a more effective filter in a relaying application, and what is the relationship between the degree of filtering and the attendant penalty in the relay response (usually a loss of operating speed)? Such an analysis has been carried out for the distance relaying application [91], and the results of that analysis will be briefly summarized in the first part of this chapter.

The remainder of this chapter will be devoted to the consideration of hardware necessary for the implementation of a digital computer relay. In this instance also the distance relay willbe taken as an example. The research team at the AEP Service Corporation with which this author is associated has been working on this application for a number of years. The first phase of this work included a joint research effort by AEP and IBM, and culminated in the development of a distance relay based upon IBM System/7 minicomputer. Standard System/7 hardware was used, and the computer was installed in an AEP substation near Roanoke, Virgina. The computer was left in the substation for about one year, and during this period several of the relaying program modules were exercised. A Standard System/7 disk was used to store transient waveform data, and was transmitted to a remote location (NY office of AEP Service Corporation) over the telephone network. The transient data was plotted on pen-and-ink plotters to generate oscillographic recordings of the transients. This phase of the AEP effort was concluded in 1974. Since then, a microcomputer based distance relay has been developed and is being tested in the laboratory at AEP, and will be further tested at a substation in the coming months. Aspects of the hardware selection procedure used in this project will be discussed.

Finally, this chapter will end with a considerable tion of the hierarchical structure of computers within a substation. Such a structure encompasses several microcomputers, a substation host computer, and communication links within the substation as well as those between the substation host computer and a remote host computer. Clearly this presentation is based upon the views of the AEP research group, and it is entirely possible that other research teams would favor a somewhat different hierarchical organization. It should be realized that as more experience is gained with the operation of microcomputers in a substation, some of the ideas presented here about the hierarchical organization may undergo modifications.

LIMITS TO RELAYING

A power system transient is a complex phenomenon. There are numerous resonance modes within a power system and the onset of a fault is usually accompanied by the oscillations of many of these resonant circuits. For certain types of faults, saturation effects further complicate the picture. In addition, fault currents may contain an exponentially decaying dc offset term which depends upon the instant of fault occurrence. Changes in system loading will affect the damping of some of the transient components. The dominant resonant modes will change as the system interconnections change due to switching operations.

It is necessary to begin with a characterization of typical power system transient waveforms. Since the frequencies of concern in most relaying applications are confined to a relatively narrow band: dc to 1 kHz, the spectral characterization might be restricted to this band. One may assume either that higher frequencies do not exist in the spectrum, or that they are eliminated by a suitable low-pass filter. The delay (phase shift) caused by such a low-pass filter is of no consequence to the relaying system. (Wave-propagation relays, which obviously deal with much higher frequencies, are excluded from the present discussion.) A convenient method of obtaining the spectrum of relay input signals (currents and voltages) is through the use of a small scale model of the relevant portion of the power system.

Figure 1 shows the one-line diagram of the system simulated in the AEP laboratory [91]. Various phase and ground faults were placed on lines 1 and 2 at different distances from bus 1. Voltages and currents at the bus 1 terminal of line 1 were recorded and their spectra obtained. System operating conditions were varied to simulate different load levels and different network configurations. In all, more than 300 fault waveforms were recorded and analyzed.

It was concluded from these experiments that by far the most significant factor affecting the signal spectrum was the total length of transmission lines connected at buses 1 and 2. Line loading, fault types etc. had a relatively minor effect on the frequency content of fault signal waveforms. For a specified system configuration, both the voltage and current waveforms contained a single dominant frequency component (besides the 60 Hz component), and the frequency of this component changed as the system configuration was changed. Since all system configurations are likely to be encountered in practice, it is appropriate to

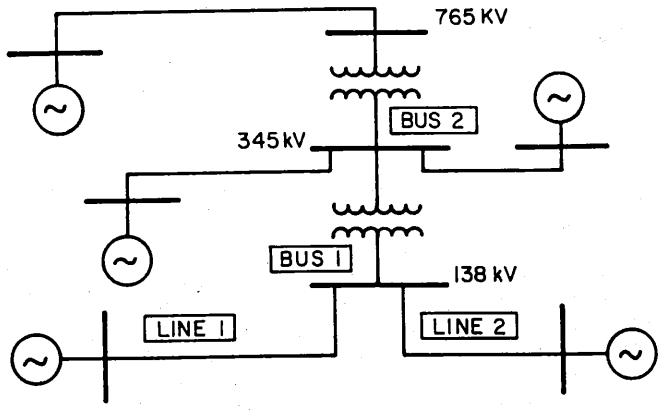


Figure 1
One-Line Diagram of the Laboratory Model System

assume that the noise (non 60 Hz components) in the fault waveforms would be an aggregate of all observed frequency components. Such a cumulative noise spectrum for the system of Figure 1 is shown in Figure 2.

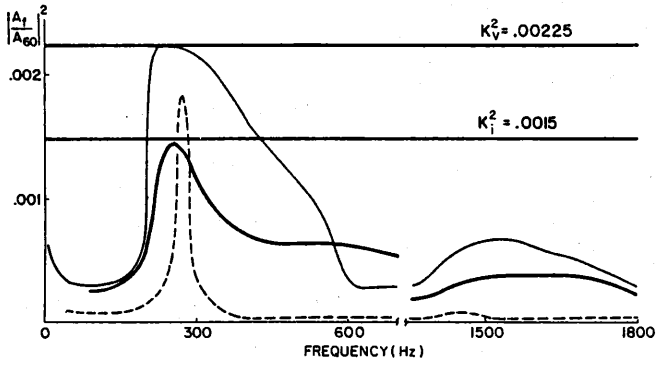


Figure 2
Spectra of Post-Fault Voltage and Current Signal Noise Components

Note that the high frequency components of the noise spectrum shown in Figure 2 are attenuated to a greater extent. This is in part due to the higher damping associated with high frequency phenomenon in the power system itself. However, to a certain extent this is also due to the fact that the system model on which measurements are made exhibits abnormally high damping at higher frequencies. Consequently, the data in Figure 2 are to be interpreted as being an indication of the scale of the noise spectrum, rather than its detailed shape or structure. For the analysis that follows, it is therefore assumed that the spectra for noise signals in the current and voltage waveforms are as described by the two horizontal level lines K_i^2 and K_v^2 respectively in Figure 2. Since these measures of the noise spectra are obtained for the specific system configuration shown in Figure 1, they are, strictly speaking, not applicable to other system configurations. Nevertheless, these spectrum levels will be considered as being representative for commonly found system configurations. Should it be necessary to be more precise in this matter, it would be necessary to conduct similar experiments on a system model with the desired configuration.

Assume that a voltage (or current) signal consists of a fundamental frequency component and a noise component as given by

$$x(t) = X \sin(\omega_o t + \theta) + n(t)$$

which can be written as

$$x(t) = X_r \sin(\omega_o t) + X_i \cos(\omega_o t) + n(t) \qquad (1)$$

where

$$\left.\begin{aligned} X_r &= X\cos\theta \\ X_i &= X\sin\theta \end{aligned}\right\} \qquad (2)$$

The noise term n(t) is assumed to have a spectrum as described by the K^2 level line in Figure 2. The time function x(t) is sampled at sampling interval (T/N) by the A/D converter, where T is the data window (i.e., a time span over which data is obtained and used to make the relaying decision), and N is the number of equally spaced samples within the period T.

$$\begin{aligned} x_k &\equiv x\left(\frac{kT}{N}\right) \\ &= X_r \sin\left(\omega_o \frac{kT}{N}\right) + X_i \cos\left(\omega_o \frac{kT}{N}\right) + n\left(\frac{kT}{N}\right) \end{aligned} \qquad (3)$$

A digital filter processes the sample set $\{x_k\}$ and produces estimates for X_r and X_i. Denoting these estimates by $\hat{X}_r$ and $\hat{X}_i$ respectively, the errors of the estimation procedure are

$$\left.\begin{aligned} p &\equiv X_r - \hat{X}_r \\ q &\equiv X_i - \hat{X}_i \end{aligned}\right\} \qquad (4)$$

The estimates are unbiased optimum estimates when

$$\left.\begin{aligned} &E\{p\} = E\{q\} = 0\,, \\ \text{and}\quad &E\{p^2\} = \sigma_p^2 \\ &E\{q^2\} = \sigma_q^2 \end{aligned}\right\} \qquad (5)$$

where σ_p^2 and σ_q^2 are minimum. The symbol $E\{\cdot\}$ in equation (5) stands for the expected value of the argument.

The solution to this optimization problem has been given in reference [91]. The optimum estimates take on a particularly attractive form when the data window T is a multiple of one-half the fundamental frequency period.

$$\left.\begin{aligned} \hat{X}_r &= \frac{2}{N}\sum x_k \sin\left(\omega_o \frac{kT}{N}\right) \\ \hat{X}_i &= \frac{2}{N}\sum x_k \cos\left(\omega_o \frac{kT}{N}\right) \end{aligned}\right\} \qquad (6)$$

when $T = m\frac{\pi}{\omega_o}$; m being an integer. Also the minimum variance of the estimates is given by

$$\sigma^2 \equiv \sigma_p^2 + \sigma_q^2 = \frac{4K^2}{T} \qquad (7)$$

where K^2 is the level of the noise spectrum as shown in Figure 2.

Consider the computation of an impedance based upon the estimation of current and voltage phasors using a data window T and the optimum estimation procedure given above. If the noise spectra for voltage and current signal noise components are described by level lines at K_v^2 and K_i^2 respectively, then variance of the impedance estimated from the current and voltage phasor estimates is given by

$$\sigma_z^2 = \sigma_v^2 + \sigma_i^2 = \frac{4}{T}(K_v^2 + K_i^2) \qquad (8)$$

where $T = m \frac{\pi}{\omega_o}$; m being an integer.

Equation (8) is the formulation of an important concept. Although in this instance the result applies to an impedance relay, the form of the result is of a general nature. It relates the uncertainty of a relay decision parameter (σ_z^2) with the level of noise in the input signal ($K_v^2 + K_i^2$) and the data window (T). Although equation (8) specifically corresponds to multiples of half-cycle data windows, results for other data windows are given in reference [91]. For the impedance relay, uncertainty of the impedance estimate determines the allowable reach-setting of the relay. Thus equation (8) can be used to obtain the relationship between the optimum reach - optimum speed settings for an impedance relay. Figure 3 shows such a curve for the impedance relay using current and voltage signals with noise components as given in Figure 2. Figure 3 (the details of its derivation can be found in the reference cited) shows that within a confidence level of 99%, an impedance relay operating in a half-cycle can not be set to reach more than 85% of the transmission line. A one cycle relay can be set to reach 90% of the line, whereas a 1/4 cycle relay can be set to reach only 60% of the line. If longer reach is attempted, the relay is likely to overreach under certain fault conditions.

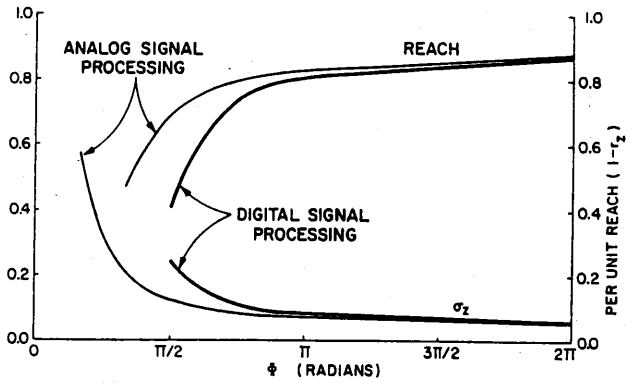


Figure 3
Optimum Speed-Reach Characteristic for an Impedance Relay

The conclusion to be drawn from the results presented in this section (and the reason for presenting them here) is that the performance of a relay is determined primarily by the nature of its input signals. Usually there are well-definable limits as to what can be achieved with a relay under optimum conditions. Such considerations help set a limit as to what can be attained by a specific realization of the relay, and in a sense provides the standard by which to judge the merit of a relaying algorithm. It is therefore of utmost importance that sufficient thought be given to analyses like this before undertaking the development of new relaying systems.

HARDWARE CONSIDERATIONS

Some of the earlier chapters have considered details of various subsystems of a computer relay. In this section of the present chapter, general requirements of a digital computer for relaying will be given. This will be followed by an example of an actual computer system being used for a distance relay application.

Refer to Figure 1 of Chapter I. It is convenient to describe the hardware requirements for the subsystems shown in that Figure as follows:

(1) Microcomputer requirements
(2) Analog Input requirements
(3) Digital Input/Output requirements
(4) Power Supply requirements

(1) Microcomputer Requirements:

The main concern in the selection of a microcomputer is the computer word length and the average instruction speed of the processor. The two most common word lengths in commercially available microcomputers are 8 bits and 16 bits. The word length may be selected based upon the requirements of the relaying algorithm. Consider a relaying algorithm which requires the execution of digital filter equations on current and voltage samples followed by a calculation of the ratio of the two filtered quantities. The value of the Least Significant Bit (LSB) β of an eight bit computer is $2^{-8} \simeq 0.004$ while that for a sixteen bit computer is $2^{-16} \simeq .000015$. A linear filter transformation on N samples of the data are subject to a maximum round-off error of $(1/2)N\beta$. If the digital filter equations require multiplications, some of which can be executed exactly in binary arithmetic, then the round-off error would be less than the estimate given above. If the computations of the filter equations is followed by a total number N_X of multiplications and divisions, the total round-off error in the result would be $(1/2)(N + N_X)\beta$. Consider for example the computation of an impedance from six samples each of voltage and current signals. The output of the filter equations is used in a complex division, which is equivalent to eight real multiplications/divisions. This would lead to a total round-off error of $(1/2)\cdot(8 + 6)\beta = 7\beta$. For an eight bit machine, this error would be about 3% whereas for a sixteen bit machine it would be about 0.01%. Considering the dynamic range of a current signal, a ratio of 20 may exist between a near-fault current and the current for a fault at the end of zone 3 reach. Thus the β in current signal processing is likely to be greater by a factor of 20. From these considerations, it is clear that to maintain the accuracy of the results of an impedance relaying algorithm within a reasonable bound of a few percent, a sixteen bit computer would be essential. Similar considerations would lead to the selection of a suitable word length for any given computational algorithm.

The necessary average instruction time of a computer can be determined from a consideration of the computational requirements of the relaying algorithm, complexity of the data management system, needs of the relaying logic programs, and the data sampling rate selected for the application. As an example, consider the distance relaying algorithm using the method of symmetrical components [69]. This application requires execution of the following approximate number of instructions in various program sections:

(a) Data Management and Symmetrical Component Computation: 300 instructions
(b) Impedance estimation: 200 instructions
(c) Relay logic: 800 instructions.

Thus the total instruction count (machine language instructions) for the execution of the symmetrical component distance relay program is about 1300 machine language instructions.

The sampling rate used in a relaying application is usually determined by the necessities of a specific algorithm and through many compromises to satisfy conflicting system needs. A sampling rate of 720 Hz has been used for most applications developed by the author's research group. This sampling rate provides a sampling interval of (1000/720) or 1.389 milliseconds. Since the relay programs are required to execute at every acquisition of a new sample set, the symmetrical component distance relay program considered above would

demand a computer with an average instruction time of about one microsecond.

Apart from the word length and average instruction time, the computer's memory system deserves special attention. There should be a facility to use Programmable Read Only Memory (PROM) for creating non-volatile program images in the computer memory. Use of PROM's should not degrade the computer processing speed. This feature produces a practical self-starting relaying program which can operate in an unattended substation and recover after a power failure. It is of course necessary to have Random Access Memory (RAM) capability for data tables and program work space requirements.

Direct Memory Access (DMA) capability for the analog input function may be a desirable feature. In particular, with computers having a relatively slow instruction time, all attempts at reducing the overhead associated with input-output functions must be made. A DMA capability in the computer would help in this regard. With bufferred A/D converters and a fast instruction set, the DMA capability is not essential for a relaying computer. All process control computers are equipped with some form of an interrupt-handling feature. This is an essential requirement, both the analog and digital input systems require an interrupt handling capability.

It is well known that a substantial effort is required to develop the software for a microprocessor based application system. The programming is generally done in an Assembler language, and every computer has its own syntax and instruction set. A versatile program development system which can be run on a mainframe computer is of considerable help in this regard. The editing, debugging and file-handling resources of the larger program development system for the microcomputer being considered for relaying application should be considered to be an essential requirement.

A certain amount of customized peripheral hardware will usually be needed in the relaying application. Examples of this are specialized arithmetic function hardware (multiply/divide), analog subsystems, digital subsystems, special communication interfaces etc. Many of these are available as standard peripheral devices on some microcomputers, nevertheless the possibility exists that some special hardware may need to be developed for the computer relaying system. To meet the requirements of customized designs, it is essential that the interface protocols of the microcomputer selected be relatively simple and accurately documented.

It is not possible to do justice to the subject of maintenance in this short chapter. Clearly, ease of maintenance is an important consideration. The circuit boards should be easily replaceable, and should preferably be available from more than one supplier. Chip level maintenance is probably not practical for most in-house maintenance organizations within a utility company, although this is probably achievable with some planning and organization. Once again, accuracy of the documentation furnished with the microcomputer system is of utmost importance.

(2) Analog Input Requirements:

The sampling rate selected for the analog digital converter is largely determined by the needs of the algorithm selected for the relaying program. As pointed out earlier, the sampling frequencies being considered for most relaying applications fall in the range of 240 Hz to 1800 Hz, with the more commonly used sampling rates being 960 Hz and 720 Hz. These sampling rates are well within the capability of the analog input peripherals available as standard options with most microcomputers. The conversion word length commonly found on these peripherals is twelve bits including the sign bit. This is perhaps one or two bits shorter than what would be desirable. The current signals from a power system have a rather wide dynamic range. The ratio of a bus fault current to a third zone boundary fault current may vary between 10 and 50. If load currents must also be processed, the dynamic range may be further extended by a factor of 2 or 3. Under these conditions the twelve bit A/D converter quantization error begins to be significant. A thirteen or fourteen bit converter may be furnished as a customized peripheral device to the microcomputer. Data capture window of most commerically available A/D converters is adequate for the relaying application. If a channel multiplexer connected to a single A/D converter is used, the channel switching time should not be so high as to cause significant data skew. The amount of data skew that can be tolerated will depend upon the specific application being considered. For an impedance relay, the phase angle accuracy in the estimate of the complex impedance (which is most directly affected by data skew error) should be of the order of 5° on a 60 Hz basis. This will require that the individual phasors must be accurate within about 2½°. This error corresponds to a maximum data skew between any pair of channels of about 100 microseconds. This requirement for a total of 7 channels is well within the capability of most A/D converters using a multiplexer. Should the actual skew be found to be greater than 100 microseconds, either separate A/D converters per channel must be used, or front-end sample- and -hold amplifiers must be used on all channels.

It is usually necessary to have a sampling rate clock available, either as a part of the A/D system, or as a separate device. The clock frequency should be adjustable in reasonably small steps. A resolution in sampling period of one microsecond should be adequate for most needs.

If the microcomputer has a DMA option available, the A/D data can be transferred to the computer memory at very high speed. In the absence of a DMA facility, the data must be transferred under program control. This latter procedure is usually not preferred as it could be quite time consuming due to the programming overhead. If the CPU time is at a premium, this could be a serious limitation. A more acceptable alternative for such cases is to use a bufferred A/D converter system. The samples obtained at each sample instant are stored in this data buffer, and transferred to the computer memory in a single I/O operation. A bufferred A/D subsystem also facilitates the intercomputer communication link with a minimum of interference with the operation of the processors. Example of such an intercomputer link will be given in a later section.

(3) Digital Input/Output Requirements:

Almost all relaying programs have modest requirements for digital input and output (I/O). A single 16 bit word is usually adequate for all the digital I/O needs of a relay. A parallel I/O port of the computer is a convenient channel for the digital I/O. Most of the digital outputs must be latched, either through program control or via external hardware latches. The computer parallel I/O is generally at TTL level, and consequently it is necessary to provide a buffer power supply and isolation circuitry for input as well as output. Optical isolation is a very effective method of achieving complete isolation between the computer and its digital I/O environment. Both the digital I/O circuits, as well as the analog input circuits must

withstand the ambient electromagnetic interference (EMI) in the substation. Surge suppression circuits, employing a combination of capacitors, zener diodes, and biased diodes are used to provide adequate surge withstand capability (SWC). As yet there are no industry standards for the testing of computer based relays in this regard; however, the standard industry test as described in IEEE standard C 37-90a may be used to prove the SWC properties of the entire relaying system. It should be recognized that this procedure may not guarantee the adequacy of surge suppression techniques being used, since a computer based relay may have modes of failure not excited by the standard C 37-90a test.

When buffer power supplies are used to power the isolated digital output circuits, a careful consideration must be given to the behaviour of these isolated circuits when the computer power goes down (and up again on reenergization). There should be no false operation of the digital output circuits under these conditions. Some special fail-safe feature may have to be incorporated in the design of the digital I/O system to avoid problems of this nature.

The digital input circuits, do not, in general, require a process-interrupt capability. However, for some special digital input points which undergo changes rather rapidly, a process-interrupt feature may become necessary.

(4) Power Supply Requirements:

It is essential that a source of power be provided for the relaying computer, such that disturbances on the ac system do not affect the computer power supply. Conventional relays are generally powered from the station battery; the usual battery voltages being 48 volts and 125 volts. Since most commercially available computers derive their power from the 117 volt system, some form of uninterruptible power supply (UPS) must be provided for the relaying computer. If the computer is adaptable to a single dc power supply (usually 5 volts dc), a dc/dc converter may be used to convert the station battery voltage to the voltage needed for the computer. This is perhaps a better option than that of using a UPS. The dc/dc converter used should not degrade the station battery bus by putting excessive switching transients on that bus. Although there are no industry standards governing this aspect of dc/dc conversion, there is general concern in the industry that the noise generated by the dc/dc converters may jeopardize other equipment in the substation which is also connected to the station battery bus.

A MICROPROCESSOR BASED DISTANCE RELAY

The general hardware considerations discussed in the previous section will now be illustrated with a specific example. It should be borne in mind that it is rare to have a commercially available microcomputer satisfy all the relaying requirements outlined above. The choosing of a computer is thus an art of finding one computer which meets most of the requirements, and then modifying the remaining requirements to obtain a compromise solution. Also because of the fast changing computer hardware scene, the optimum choice at a given time may not be the best choice a few years hence.

The distance relay computer system being described here has undergone successful laboratory testing, and is scheduled for field-testing in an AEP system substation in April 1979. The distance relay uses an algorithm based upon the method of symmetrical components [69,94]. However, the details of the algorithm do not critically affect the selection of the microcomputer. The computer chosen for this application is the PLESSEY MIPROC-16 microcomputer, and meets a majority of the requirements discussed earlier. The PLESSEY was selected after a detailed evaluation of microcomputers commercially available in 1977-78. This is a 16 bit computer using two separate memories for programs and data. The basic CPU cycle time for the high-speed version is 250 nanoseconds. An eight level priority interrupt system is built into the hardware, and a total of 256 priority sublevels can be provided through a grouped or daisy-chain connection between interrupting peripherals. A DMA interface is available, although it was considered to be unnecessary for the distance relaying program because of the relatively high speed of the computer. A maximum of 64 K words of data and program memories can be accommodated. The relay computer is provided with 8 K words of data and program memory.

Multiply and divide instructions are microcoded resulting in execution times of between 16-32 CPU cycles. Most other instructions execute in 1 CPU cycle. A hardware multiply board is available as a standard peripheral. Using this option, two 16 bit words can be multiplied with four instructions, using 4 CPU cycles. No hardware divide option is available. Normal serial and parallel I/O peripherals are available as standard options. Program development software suitable for commonly used host systems is a standard feature of its software support system.

Figure 4 shows the functional blocks of the distance relay system. The power supply consists of a dc/dc converter (not supplied with PLESSEY) which converts the station battery power from 125 volts to the 5 volts level needed by the computer. The standard PLESSEY power supply is from the 117 volts ac source. The high speed memory units (75 nanosecond access time) require substantial power input. A full complement of peripherals needed for the relaying application requires a nominal power input of 200 watts.

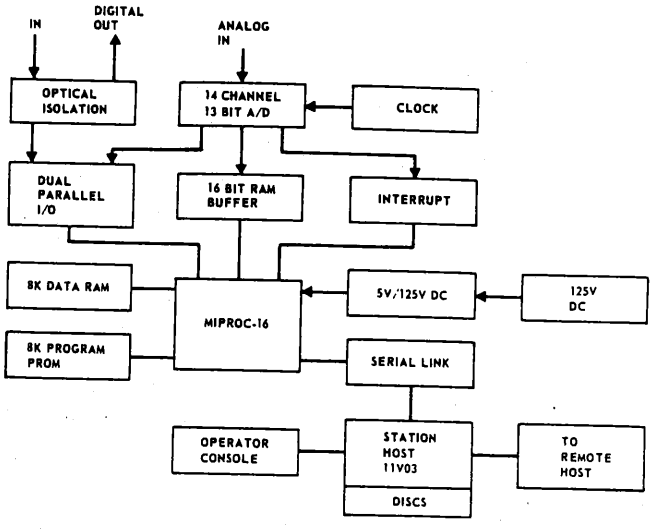


Figure 4
Microcomputer Based Symmetrical Component Distance Relay

Two alternative analog input systems were designed for this application.* Both systems use a 16 x 16 word RAM buffer where a complete sample set is stored. The sample set consists of samples of (V_a, V_b, V_c, I_a, I_b, I_c, I_o) of the protected line, and also samples of the

*The analog input systems have been designed by Messers. J. Gohari, J. Jauch, and A. Otis of AEP Service Corporation, NY.

same signals attenuated by a factor of 0.866. This constant is the irrational Fourier coefficient associated with a sampling rate of 720 Hz selected for this application. One A/D system uses seven 8 bit A/D converters, whose range is magnified by an auto-ranging circuit, so that a net dynamic range of 12 bits plus the sign bit is obtained. The non-attenuated signals are sampled first, followed by a sample set of the attenuated signals. When the 14 data values are accumulated in the RAM buffer, the processor is interrupted, and the data is transferred to the main data memory under program control.

The second A/D converter system uses a single A/D converter with a 16 channel multiplexer. The word length of this scheme is also 12 bits. The multiplexed system has fewer IC chips than the multiple A/D converter system described above. Both of these systems will undergo field testing to evaluate their reliability, stability under field conditions, etc.

The analog and digital signal interfaces have also been designed by AEP engineers.† The current signals are isolated with an isolating transformer. Anti-aliasing filters designed for a cutoff frequency of 360 Hz are active filters having a transfer function of the form $(a_1/\{s^2 + a_2 s + a_3\})$ where the a's are design constants. The output of these filters is connected to an active circuit representation of the mimic circuit. This is a circuit having a transfer function of the form $(1 + sT)$ where T, the time constant, matches the power system time constant. The phase current mimic circuits are matched to the positive sequence time constant whereas the zero sequence current mimic circuit matches the zero sequence time constant of the power system. The output of these circuits is limited to about ±8 volts for maximum fault current, ±10 volts being the maximum signal input capability of the A/D system.

The voltage signals are obtained from a potential divider connected to the secondary of line-side CCVT's. Station surge isolation is provided by capacitors and reverse biased diodes connected across the input lines. Anti-aliasing filters similar to those used for current input signals are used for voltage signals also. The output of the filters is limited to ±8 volts during normal system voltage conditions.

The digital input/output circuits provide a TTL level interface to the computer, and optically isolated bufferred switches are available for external connections. One port of the dual port parallel I/O board of the PLESSEY is used for digital I/O, while the other port is used for analog data input. The process interrupt feature is not used for the digital inputs.

For the initial phase of field testing of the distance relay, a host computer will be used to handle external communications and to collect the historical data files from the relay computer. A PDP 11 V03 with a dual floppy disk system is used as a host computer. It is connected to the PLESSEY by a 9600 baud asynchronous serial link. The host computer initiates data transfer from the relay computer when requested by the latter to do so. A typewriter terminal provides access to the host as well as to the relay computer. The operation of the relay computer can be monitored from this operator's console of the host computer. As mentioned previously, this relay-host computer system will undergo field-testing in the coming months.

†The interface circuits have been designed by R. Haas, AEP Service Corporation, Canton.

A HIERARCHICAL STRUCTURE FOR SUBSTATION COMPUTERS

It has been mentioned earlier that all the substation protection, control, alarm, and data logging functions can be handled by dedicated microprocessors. These multiple computers should be considered to be members of a hierarchical computer system within the substation. Such a structured arrangement leads to many potential benefits, and helps identify the requirements and limitations of the inter-computer communication links.

Figure 5 shows the hierarchical structure for computers in an EHV substation. R_1, R_2, ... etc. are relaying computers dedicated to the protection functions of various power system components in the substation. For certain protection tasks, where redundancy through duplication is required, a second relaying computer may be dedicated for the back-up task as in conventional relaying. It may be possible to share a single back-up relaying computer between several primary relaying systems. P_1, P_2, ... etc. are the peripheral systems of each computer. For the relaying computer, the peripheral system consists of the analog input system and the digital input/output system. Each relaying computer with its peripheral equipment constitutes a dedicated protection system. These dedicated systems do not depend on any other system within the substation. Failures within any other system in the substation do not affect the performance of a protection system.

Several of these relaying systems use input signals which are also used by some other relaying systems. Examples of this are current signals used by a bus relay, which are also used by feeder or transformer relays connected to that bus. Similarly, all the relays protecting transmission lines which originate from the same bus use identical voltage signals. The computer system shown in Figure 5 is capable of providing an added level of redundancy whenever two or more relaying systems use identical input signals. Samples obtained by one relaying computer could be made available to another computer if its input system fails. One method of sharing the data samples would be to

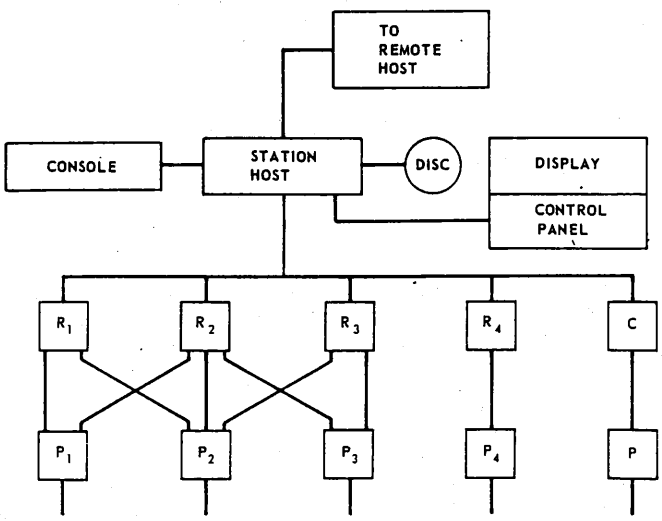


Figure 5
Hierarchical Structure for Substation Computers

provide each relaying computer with a multiple port memory. However, in the current technology such

memories are not commercially available. The data volume of sampled data is such that normal teleprocessing communication links between processors with their attendant software overheads would not be a practical means of data exchange in this case.

The bufferred peripheral device as discussed earlier provides a practical method of obtaining the redundant data paths. It is possible to provide a sufficient number of parallel I/O ports for each processor, and connect them to the appropriate peripheral device buffers. During normal operation, these alternate data paths would be unused. However, upon the failure of its dedicated peripheral device (it is of course necessary to detect this failure) the affected relaying computer would activate the alternate data paths under program control. One may consider this to be an added level of redundancy for the protection system; or for a given level of redundancy requirement for the entire system eliminate certain duplicate back-up protection systems. Relaying computers R_1, R_2, and R_3 are shown linked in this fashion in Figure 5. Note that these links are non-essential for the operation of R_1, R_2, R_3 during normal system conditions, but provide an additional data path for certain hardware failures. Of course, some relays may not share their data with any other relay, and in this case a stand-alone relay, such as R_4, is used.

Computer C and its peripheral P are dedicated to the data logging, alarm monitoring, and control function. Certain of these functions may reside in the relay computers themselves. For example, controlling the circuit breakers of a line can be done through the line relay. Similarly, voltages and power flow on the line can be computed from the sampled data, provided a sufficient resolution can be designed into the current input channels. The control and data logging functions not covered by any of the relaying computers are handled by the computer C.

All the relaying and control and monitoring computers are connected to the station host computer through a teleprocessing link. Since data transfer over this link is at a much slower rate, a conventional serial link is considered to be adequate for this function. The host computer handles the protocol of communication over this link, and each of the microcomputers contains a rudimentary interface software to handle their end of the communication protocol. Apart from the control signals which originate at the host computer, historical data files stored by each of the microcomputers are transferred to the host over this communication link.

The host computer, which is also based on a microprocessor, has a bulk storage capacity; flexible disks being considered at present for this function. In addition, a programmer's console is connected to the host. This will be used for software checks and maintenance by computer programming personnel. The substation maintenance personnel will access the system through a control and display panel. The display may vary from simple meter read-out panels to a dynamic one-line diagram of the station on a CRT screen. The control panel may consist of a key-pad for specific information retrieval request and various control commands. Control commands will have echoing or check-back features, as well as an execution confirmation phase wherever possible.

The host computer will have a teleprocessing link to a remote host computer, which may be used for data transfer in either direction, as well as for remote control signals. The wave-form data collected by the relay computers may be displayed as an oscillograph either locally, or at a remote location. Sequence-of-event analysis, or post fault analysis can be similarly provided either at the remote host or at the local station host upon request by an operator.

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CHAPTER IX

BIBLIOGRAPHY OF DIGITAL COMPUTER RELAYING LITERATURE

References quoted in Chapters I through VIII are listed in a chronological order in this chapter. Publications on the subject of Computer Relaying which are easily retrievable and are in English have been included. Some references on other topics discussed in this text, are also recorded. No bibliography is complete and this one is no exception. An attempt has, however, been made to include all important references on power system protection by programmable digital devices.

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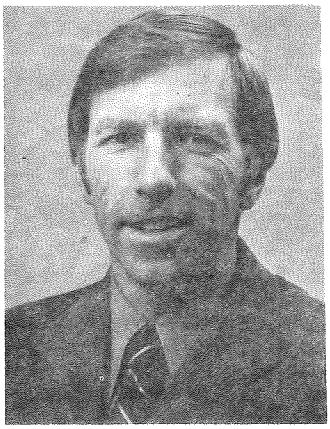
BIOGRAPHIES OF CONTRIBUTORS



Thomas C. Baird (M '60) was born in Omaha, Nebraska, on February 15, 1935. He received the BSEE degree from the University of Colorado in 1957 and the ME degree from Iowa State University in 1976.

For most of his professional life he was relay engineer with Iowa Power and Light Company in Des Moines, Iowa, and is presently Supervisor of Planning.

He is a member of the IEEE Power Engineering Society, Eta Kappa Nu and Tau Beta Pi, and is a Registered Professional Engineer in the State of Iowa.

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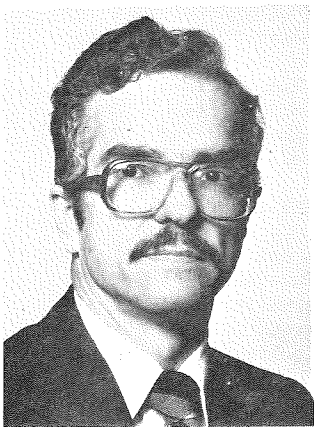
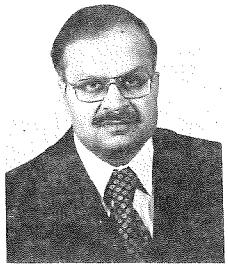
He joined the General Electric Company in 1951 and has been employed at their Switchgear Plant in Philadelphia since 1954. He has worked in circuit breaker research and the application of mathematics and computers to switchgear products.

He is presently a member of the IEEE Power System Relaying Committee and the Computer Relaying Subcommittee.

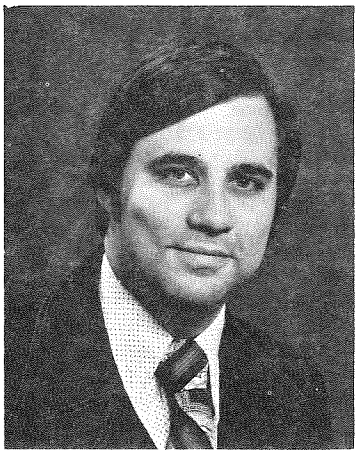


Cyrus O. Harbourt (M '59) was born in Baton Rouge, Louisiana in 1931. He holds BS, SM, and Ph.D. degrees in Electrical Engineering from Louisiana State, Massachusetts Institute of Technology, and Syracuse University, respectively. He has taught electrical engineering at Syracuse, the University of Texas at Austin, and the University of Missouri-Columbia, where he is currently Professor of Electrical Engineering.

Dr. Harbourt served as Chairman of Electrical Engineering at UMC from 1967 to 1977. He spent 1977-1978 with Bonneville Power Administration in Portland, OR, in the Branch of Substation and Control Engineering, where he worked on a variety of projects in computer relaying and power system instrumentation.



Arun G. Phadke: Consulting Engineer, American Electric Power Service Corporation, New York. Dr. Phadke received a B.Sc. degree in Mathematics and Physics from Agra University, and the B. Tech. (hons) in Electrical Engineering from the Indian Institute of Technology, Khargpur, in 1955 and 1959, respectively. He received his M.S. and Ph.D. degrees in Electrical Engineering from the Illinois Institute of Technology, Chicago and the University of Wisconsin, Madison in 1961 and 1964, respectively. He was a Systems Engineer with Allis-Chalmers Co., Milwaukee from 1963 to 1967. During this period, he was active in the design and construction of the AC/DC Network Simulator Facility, which was funded by the Edison Electric Institute, at the University of Wisconsin, Madison. He was an Assistant Professor of Electrical Engineering at that University from 1967 to 1969. He has been working with the American Electric Power Service Corporation, New York since 1969. His work at AEP is concerned with application of computers in all branches of power system engineering. He was a Visiting Professor at VPI and SU, Blacksburg, Virginia during the academic year 1978-79.



B. Don Russell (M,70) was born in Denison, Texas. He received the B.S. and M.E. in electrical engineering from Texas A & M University, College Station, Texas in 1970,1971 respectively. He received the Ph.D. degree in electrical engineering from the University of Oklahoma in 1975.

In 1976 he joined the teaching faculty of Texas A & M and is presently an Associate Professor of Electrical Engineering. He is also a Research Administrator with the Electric Power Institute at TAMU. Dr. Russell's present research includes investigation of the electromagnetic environment in substations, design of a distribution high impedance fault detector, and the development of microcomputer based substation automation systems.

Dr. Russell is Associate Editor of the journal Electric Power Systems Research. He recently edited the book Power System Control and Protection, Academic Press. Dr. Russell was recently named Young Engineer of the Year by the Brazos Chapter, Texas Society of Professional Engineers, Eta Kappa Nu, Tau Beta Pi, Sigma Pi Sigma, and is a Registered Professional Engineer in Texas.

Mohindar S. Sachdev (M'67, SM'73) was born in Amritsar, India, in 1928. He received the B.Sc. Engineering degree from the Benares Hindu University, Benares, India, the M.Sc. degrees in Electrical Engineering from the Panjab University, Chandigarh, India and the University of Saskatchewan, Saskatoon and the Ph.D. Degree from the University of Saskatchewan, Saskatoon, Canada.

In 1951 he joined the Punjab P.W.D. Electricity Branch and worked in distribution system operation and management until 1958. He was then Assistant Resident Engineer of the Uhl River Hydroelectric power plant at Joginder Nagar, India, during 1959 and later worked for two years at the Bhakra Power Plant I on the design of control circuits and co-ordination of the plant equipment. His services were then loaned to the Punjab Engineering College, Chandigarh, India, where he was an Associate Professor until 1965.

He joined the Faculty of Engineering at the University of Saskatchewan in 1968 where he is presently Professor of Electrical Engineering, Chairman of the Research and Graduate Studies Committee and a member of the Power Systems Research Group. His areas of interest are Power System Analysis, High Voltage DC Transmission and Power System Protection.

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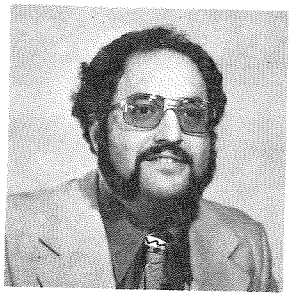
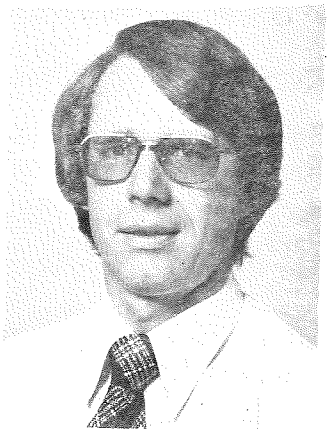


Eric A. Udren received his BSEE degree with Honor from Michigan State University in 1969. He joined the Graduate Student Program of Westinghouse Electric Corporation, and was assigned to the Relay-Instrument Division in Newark, N.J. There he was engaged in software development for the Prodar 70 experimental computer relaying project. From 1972 to 1977, he was an applications consultant for several lines of conventional protective relays; and also pursued continuing computer relaying devlopments including a joint sudy of computer-relaying technology by Westinghouse and Pennsylvania Power & Light Company. In 1977, Mr. Udren received the Westinghouse B.G. Lamme scholarship, with which he completed a one-year graduate research program in electrical engineering at the University of Cambridge, U.K. He subsequently located at the Westinghouse Research and Development Center in Pittsburgh, where he is currently engaged in protection-subsystem development efforts for the Transmission-Substation Control and Protection System Project sponsored by the Electric Power Research Institute.

Mr. Udren is also pursuing an MSEE degree at New Jersey Institute of Technology, Newark, N.J. He is a member of the IEEE Power Engineering Society and of the Power System Relaying Committee, where he has held Working-Group Chairman and Liaison posts.



Lewis N. Walker is currently an Associate Professor of electrical engineering at the University of Missouri-Columbia, specializing in the analysis, design, modeling and computer control of electric power systems. He directs the Digital Power Research Group and is Co-Director of the Energy Systems and Resources Program. He received the BSEE, MSEE and Ph.D. degrees from the University of Missouri-Columbia.

Dr. Walker has authored and co-authored several technical articles and presentations concerning the application of digital computers to the on-line control of electric power systems. The Digital Power Research Group developed a hybrid simulator of electric power systems under sponsorship of the Electric Power Research Institute to study the long term dynamic response of power systems. The simulator is currently being adapted for use in dispatch operator training short courses and is being used for various research studies in power system planning and operation.

He is currently a member of the IEEE relaying committee and serves as chairman of the Line Protection Working Group of the relaying committee. He is a member of ASEE, IEEE, Eta Kappa Nu, Sigma Xi and is President of the Central Chapter of the Missouri Society of Professional Engineers.